Uranus_KLS_N17P

Schematics Document

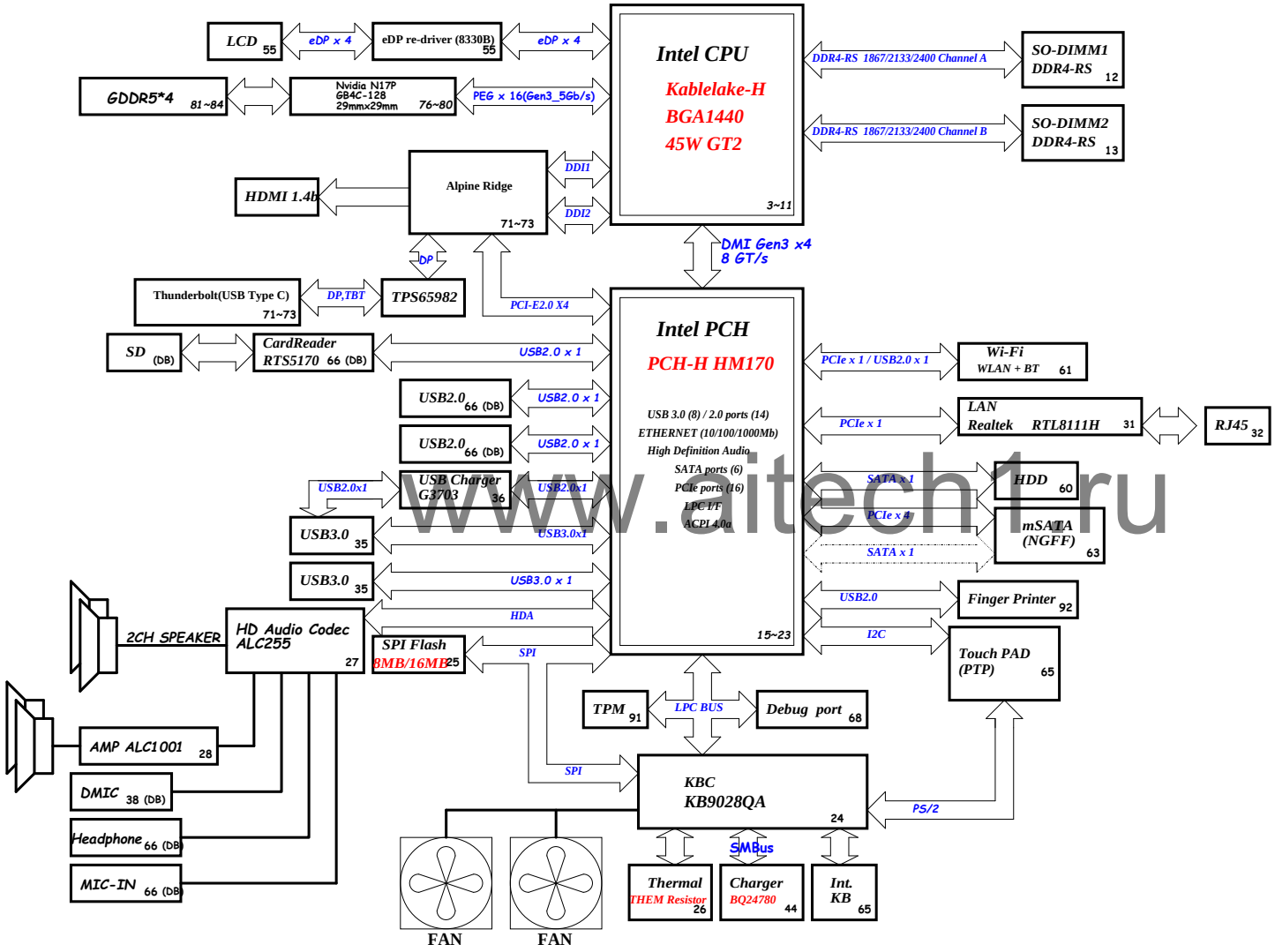
SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A	Document Number: Uranus_KLS	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 1 of 105	

Uranus_KLS_N17P Board Block Diagram

Project code : 4PD0BP010001
PCB P/N : 16585



CHARGER BQ24780SRUYR 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT6575D 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power ISL95855HRTZ 46,47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

DDR4 power APW8861QBI-TRG 51	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 2D5V_S3 0D6V_S0

1D0V_S5 RT8231AGQW 52	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

CPU 1D8V_S0 RT9025 53	
INPUTS	OUTPUTS
3D3V_S5 5V_S5	1D5V_S0

Switches 40	
INPUTS	OUTPUTS
5V_S5 3D3V_S5 1D0V_S5	5V_S0 3D3V_S0 0D95V_VCCIO 1V_VCCST

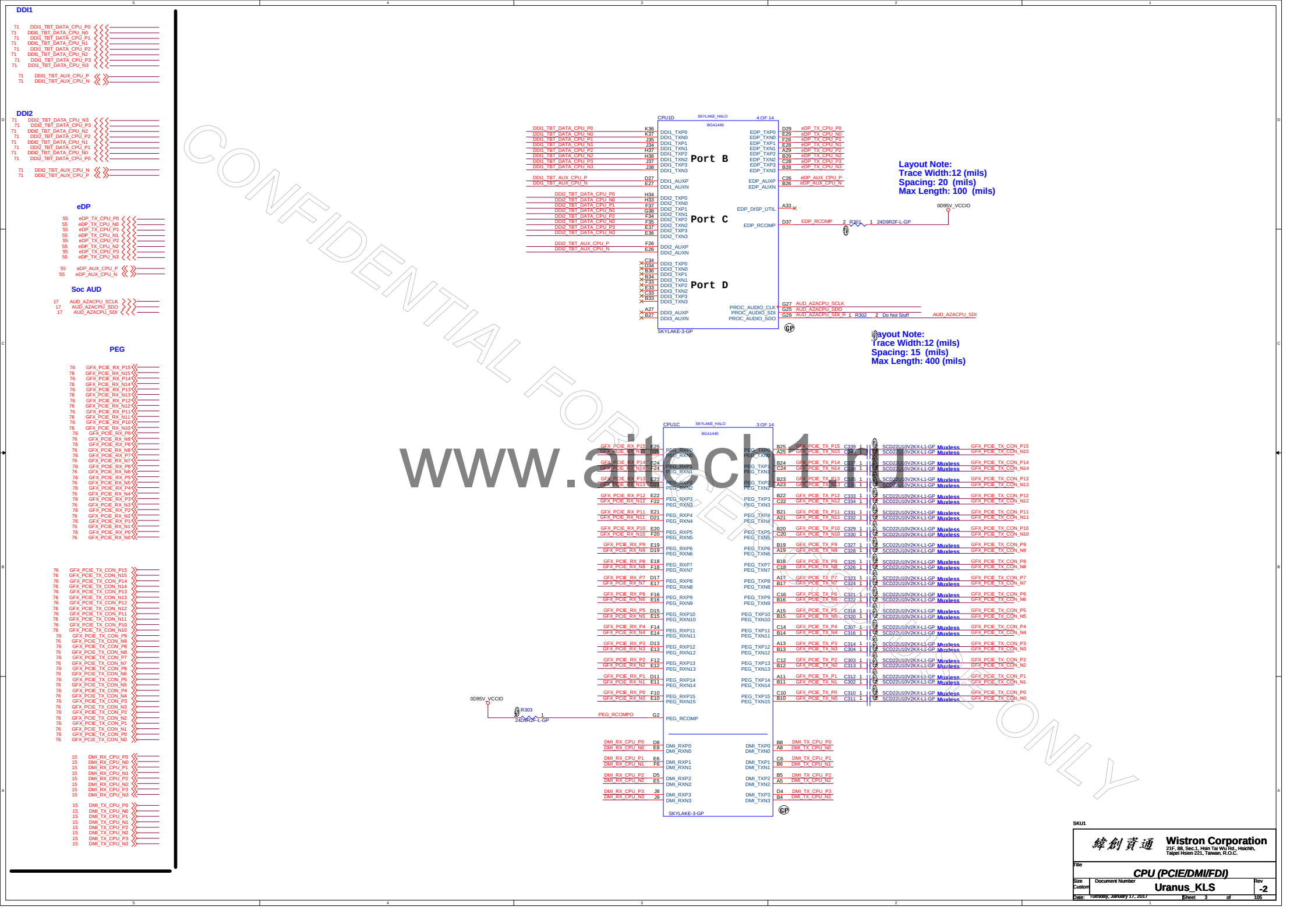
SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size: C | Document Number: Uranus_KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 2 of 105



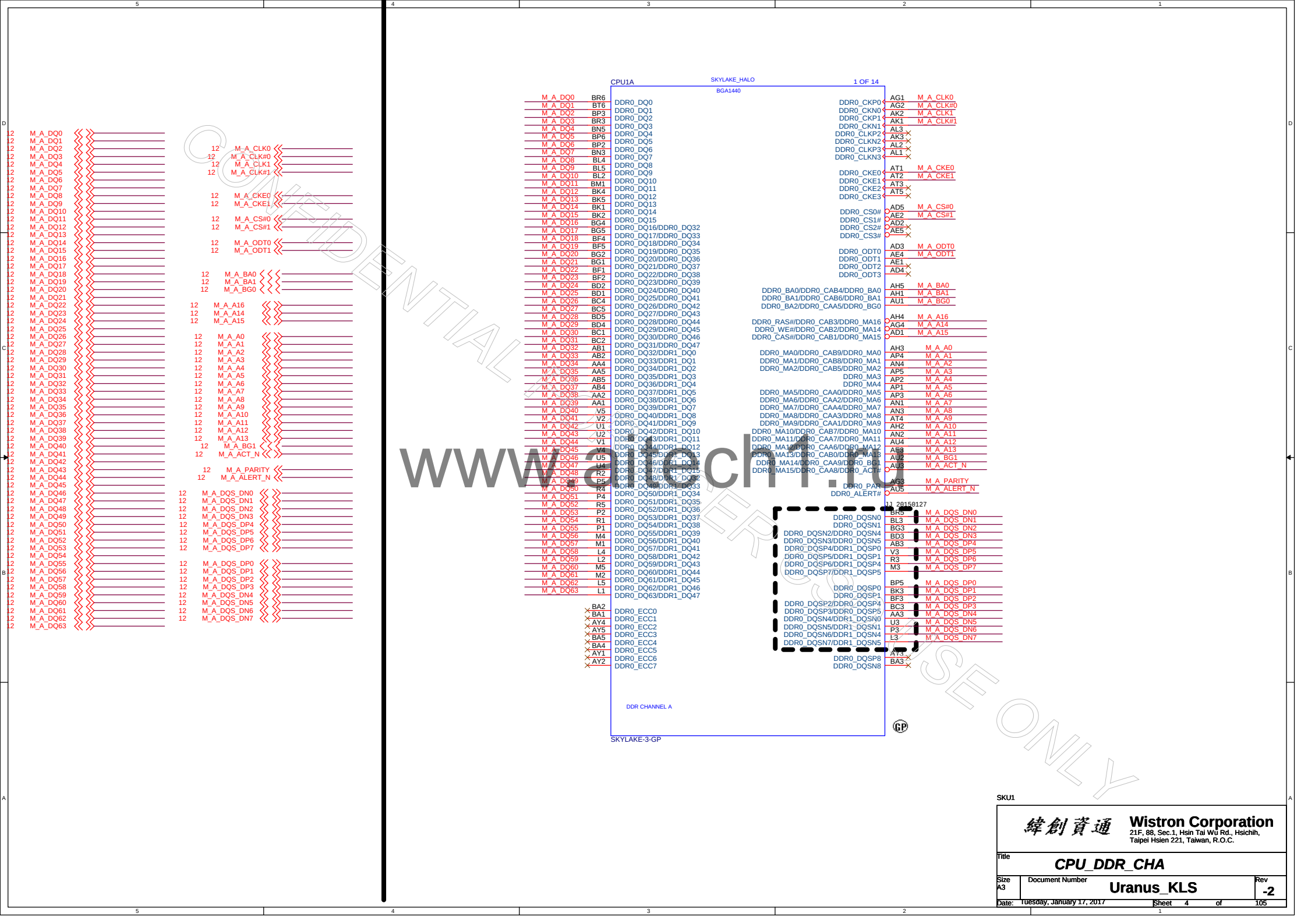
SKU1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
Custom	Uranus_KLS	-2

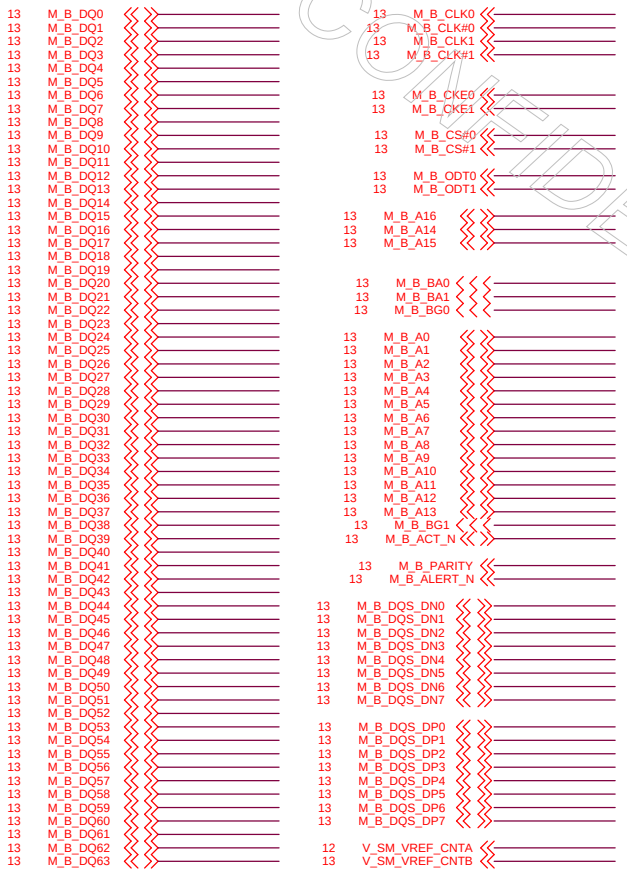
Date: Tuesday, January 17, 2017 Sheet 3 of 105

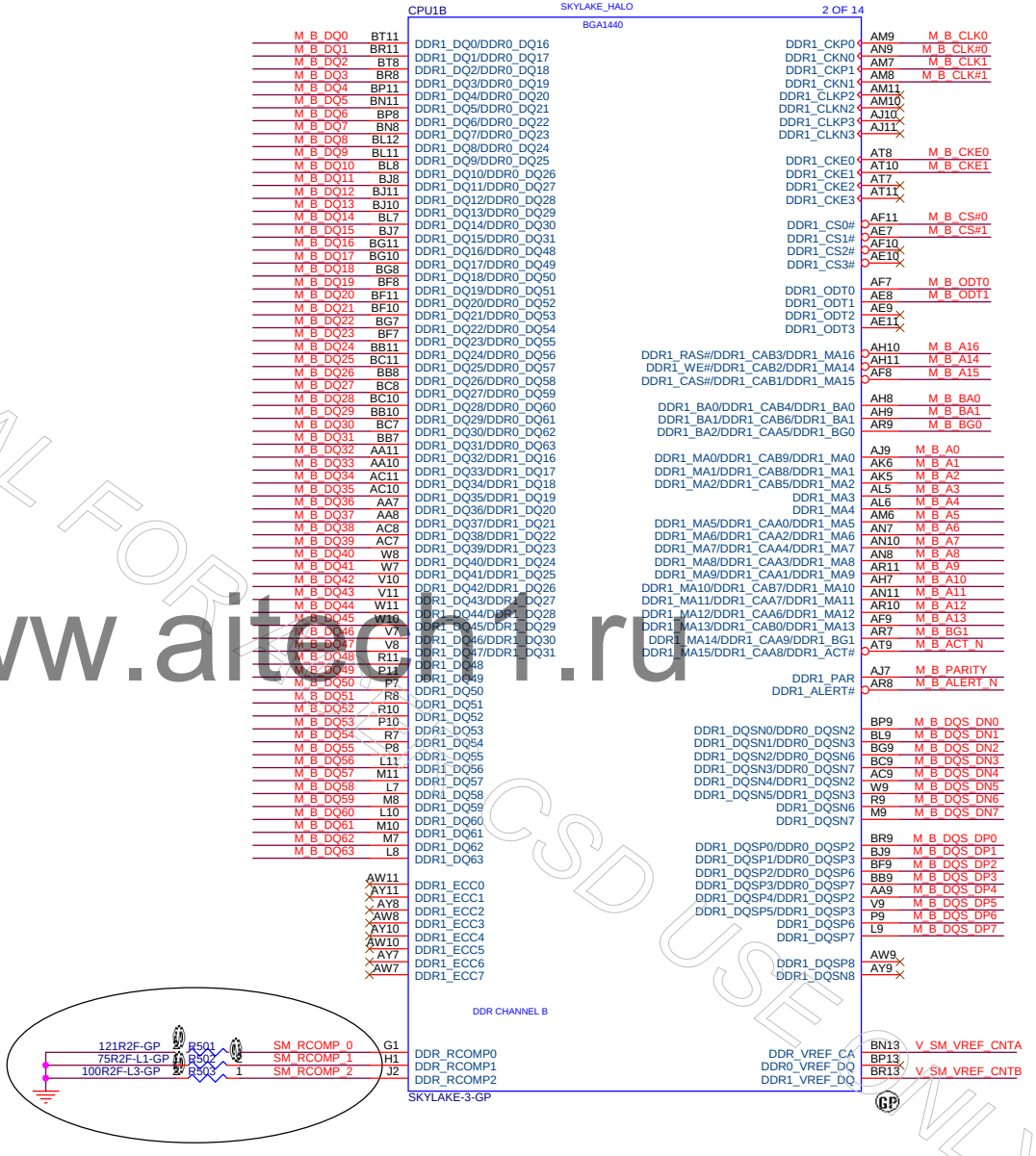


SKU1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU_DDR_CHA***	
Size A3	Document Number **Uranus_KLS**	Rev **-2**
Date: Tuesday, January 17, 2017	Sheet 4 of 105	

SSID = CPU

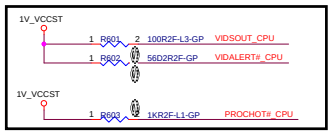


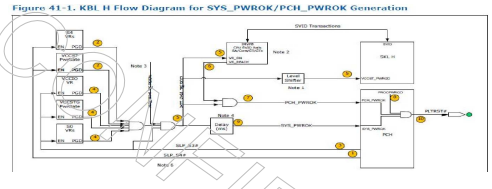


SKU1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU_DDR_CHB***	
Size A3	Document Number **Uranus_KLS**	Rev -2
Date: Tuesday, January 17, 2017	Sheet 5 of 105	

AROUND_CPU





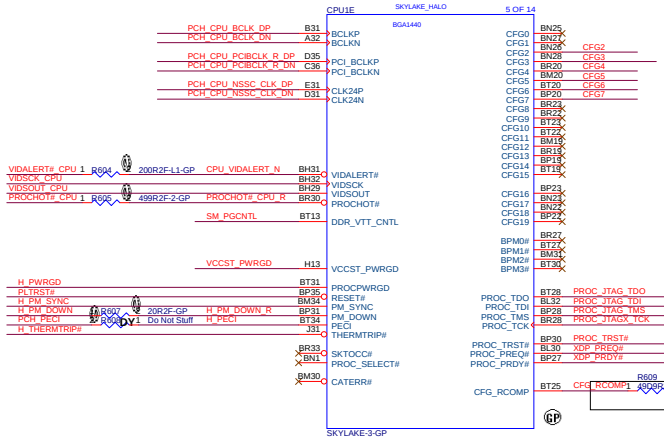
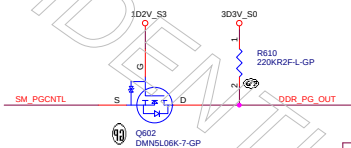
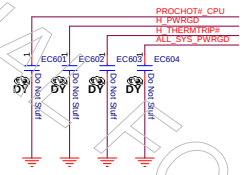


Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

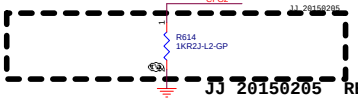


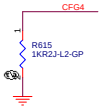


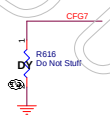
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

eDP Enable	
CFG4	1:Disable 0:Enable

PEG Training	
CFG7	1:(default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training.







PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Internal Pull-Up / Pull-Down Terminations

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	$V_{CC_{IO}}$	16-60 Ω
PREQ# |	Pull Up	$V_{CC_{ST}}$	3 kΩ
PROC_TDI	Pull Up	$V_{CC_{STG}}$[1]	3 kΩ
PROC_TMS	Pull Up	$V_{CC_{SGT}}$[1]	3 kΩ
CFG[19:0]	Pull Up	$V_{CC_{IO}}$	3 kΩ

Note:
1. For SKL-S it should be $V_{CC_{ST}}$

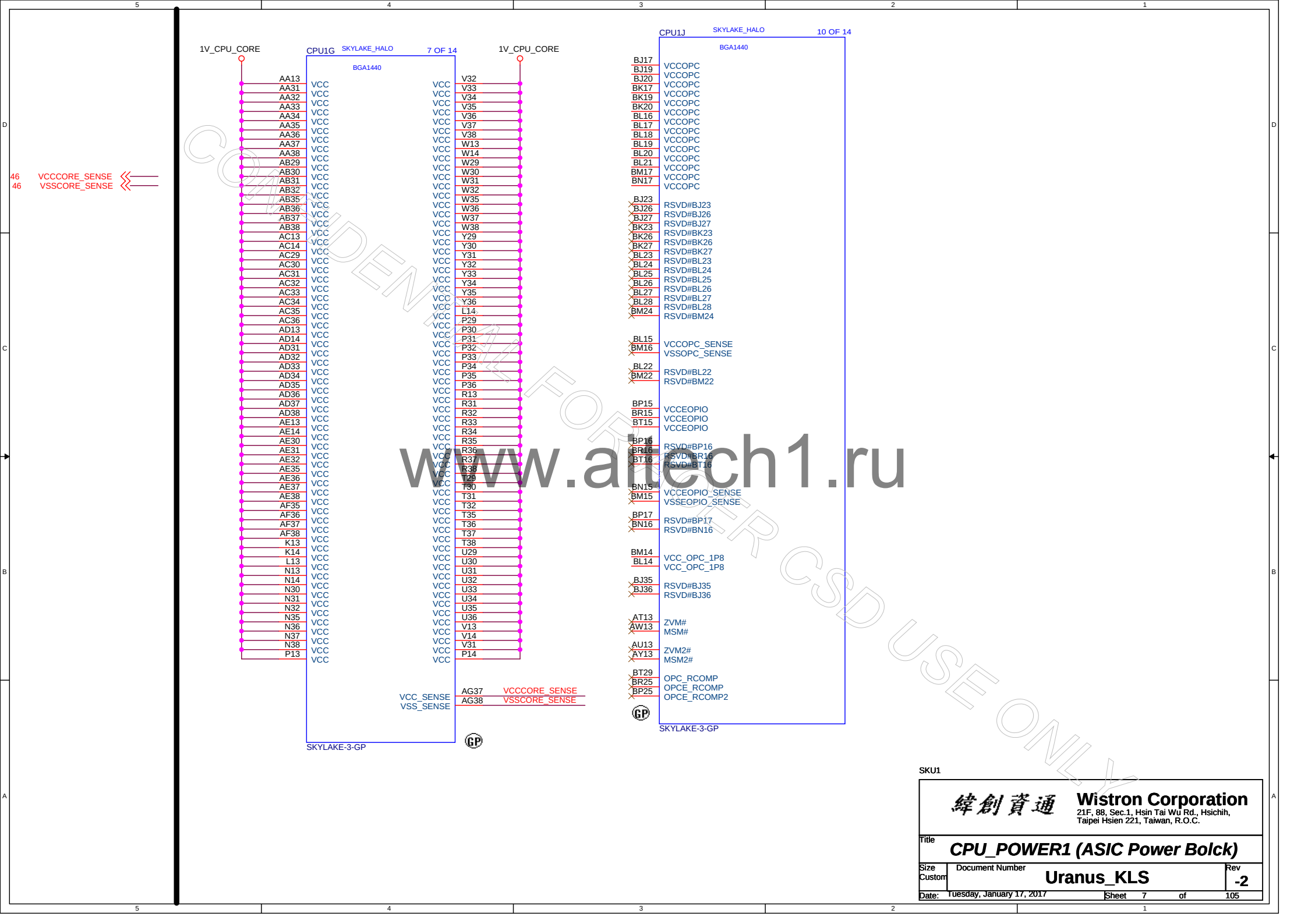
SKU1

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_CFG_CFG STRAP

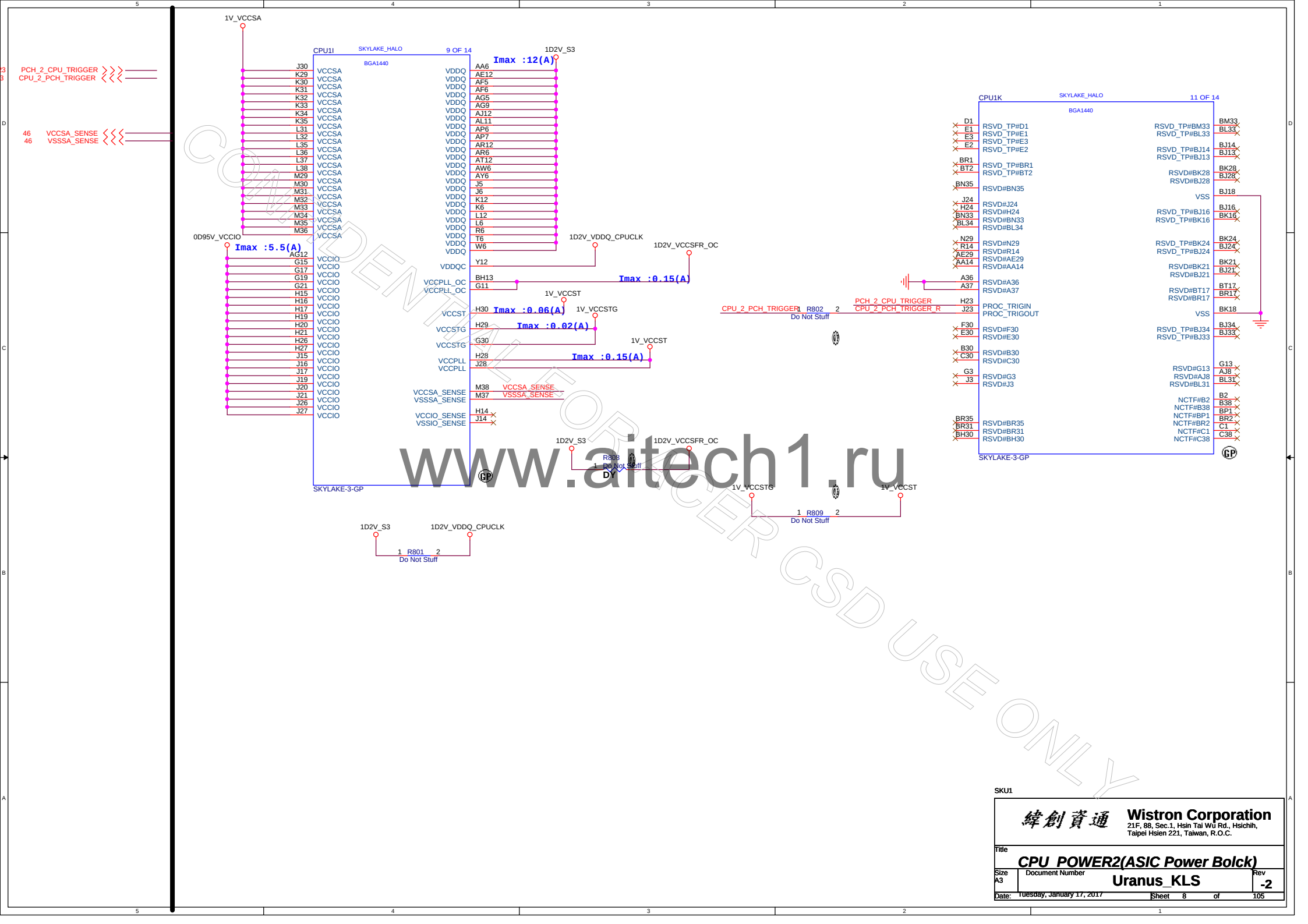
Size: A2 | Document Number: Uranus_KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 8 of 105



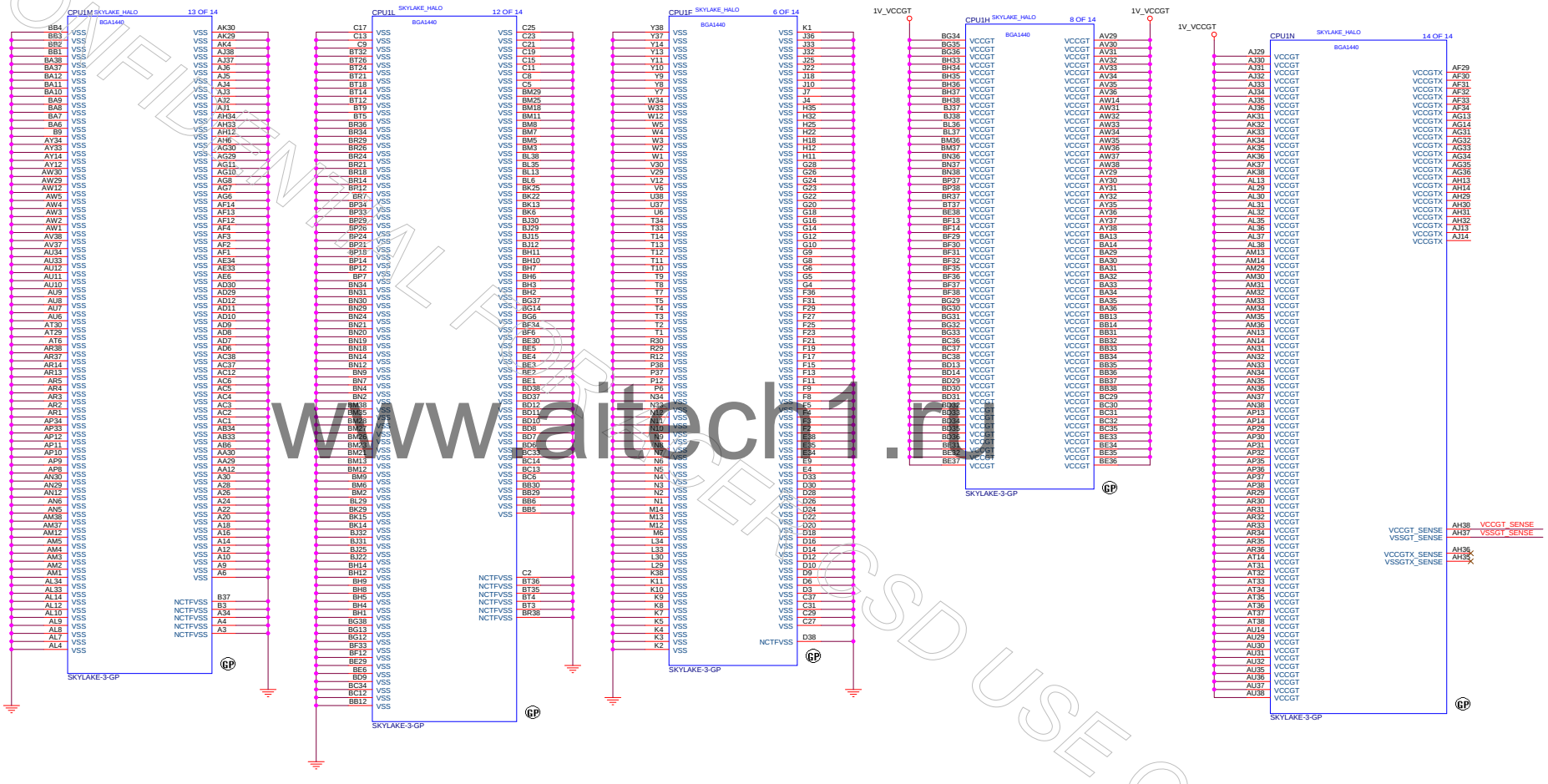
SKU1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU_POWER1 (ASIC Power Bolck)***	
Size: Custom	Document Number: **Uranus_KLS**	Rev: **-2**
Date: Tuesday, January 17, 2017	Sheet 7 of 105	



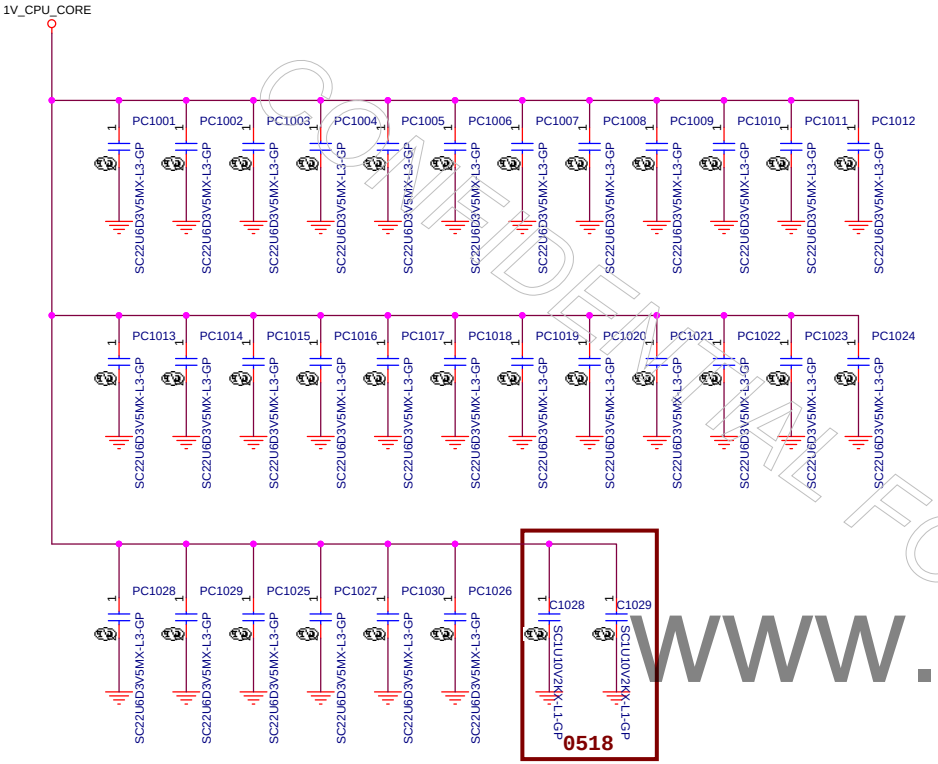
SSID = CPU

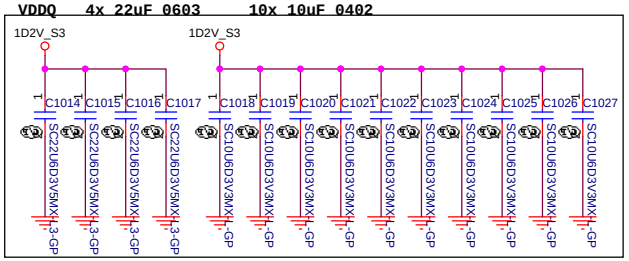
VCCGT_SENSE 46
VSSGT_SENSE 46

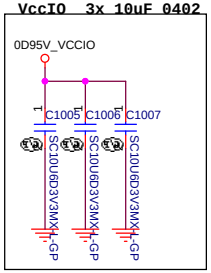


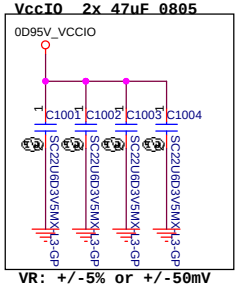
SKU1

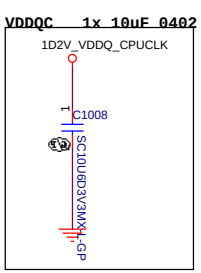
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU_POWER3(ASIC Power Bolck)	
Size: Custom	Document Number: Uranus_KLS	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 9 of 105	

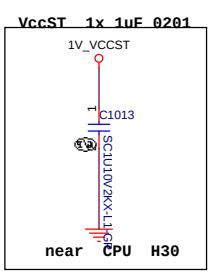




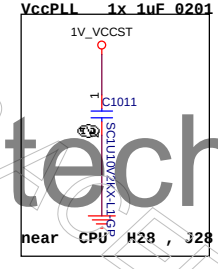


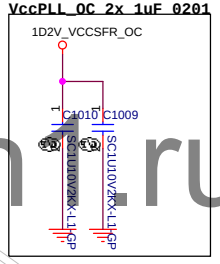


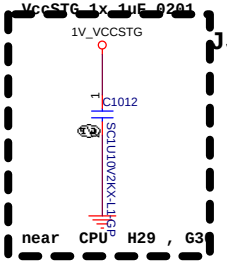




VR: +/-5% or +/-50mV
Place close to VR output







JJ 20150130

Table 49-3. Decoupling Requirements for KBL H Processor

Domain	Board Edge cap	Backside cap	Notes
Vcc	4x 47uF 0805		
		8x 22uF 0603	
		28x 10uF 0402	
		63x 1uF 0201	
Vcc_{GT}	6x 47uF 0805		
		8x 22uF 0603	
		35x 10uF 0402	
		68x 1uF 0201	
Vcc_{GTx}	8x 22uF 0603		Only needed when supporting 44e
		4x 10uF 0402	Only needed when supporting 44e
		12x 1uF 0201	Only needed when supporting 44e
Vcc_{SA}	1x 47uF 0805		
		1x 47uF 0805	
		7x 10uF 0402	
		3x 1uF 0201	
V_{DDQ}		4x 22uF 0603	
		10x 10uF 0402	
V_{DDQC}		1x 10uF 0402	
Vcc_{IO}		3x 10uF 0402	
Vcc_{ST}		1x 1uF 0201	Do not route Vcc_{GT} closest adjacent layer over any power net other than ground.
Vcc_{STG}		1x 1uF 0201	Share supply with 1.0V PCH rail
Vcc_{PLL}		1x 1uF 0201	Do not route Vcc_{PLL}, Vcc_{STG} closest adjacent layer over any power net other than ground.
Vcc_{PLL_OC}		2x 1uF 0201	Share with VDDQ, Do not route Vcc_{PLL_OC} closest adjacent layer over any power net other than ground.
Vcc_{DPC}		10x 10uF 0402	Only needed when supporting 44e VR: +/-5% or +/-50mV
Vcc_{EOPIO}		3x 10uF 0402	Only needed when supporting 44e VR: +/-5% or +/-50mV

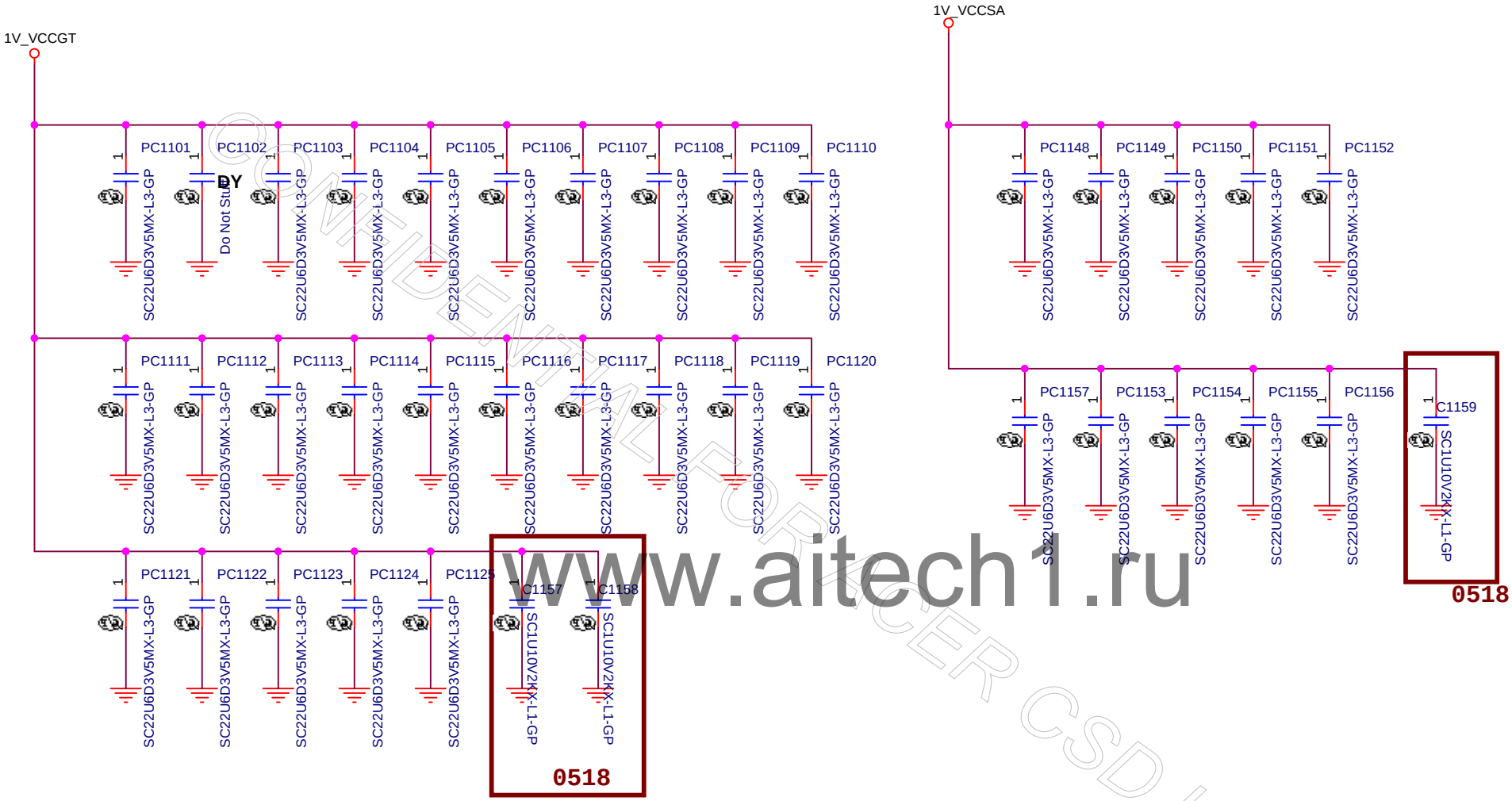
SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 010 CPU (Power CAP1)

Size	Document Number	Rev
A3	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 10 of 105



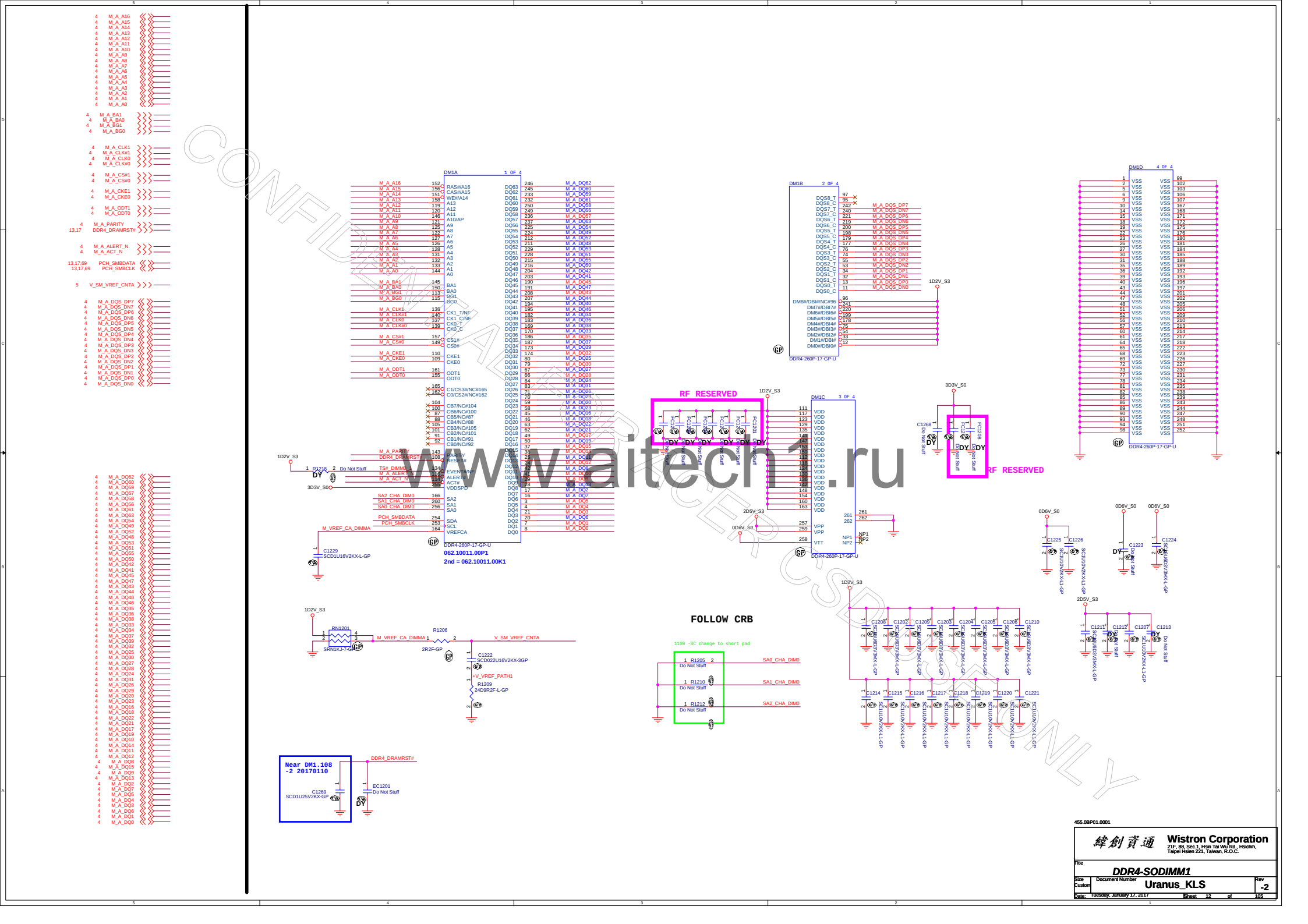
SKU1

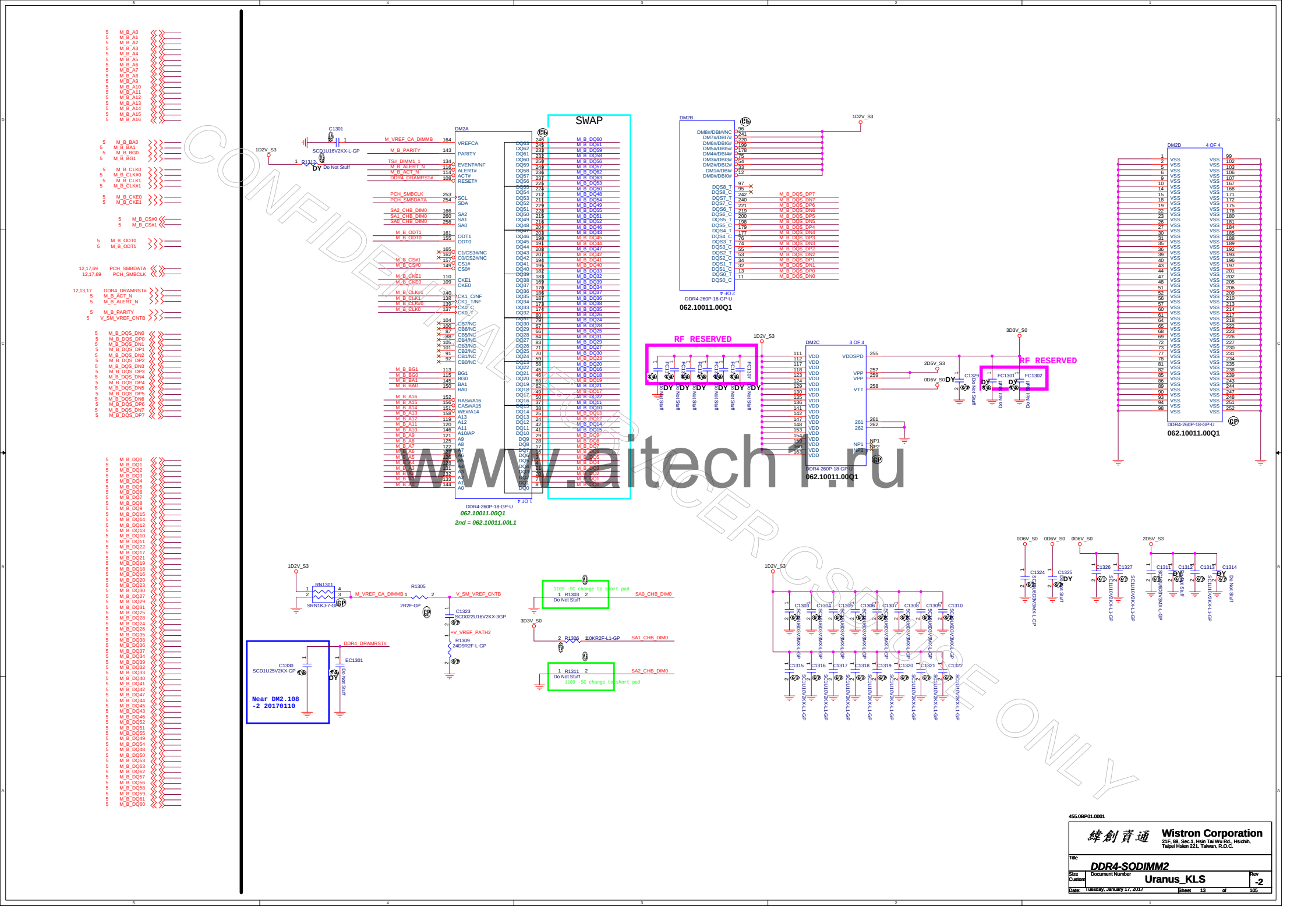
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

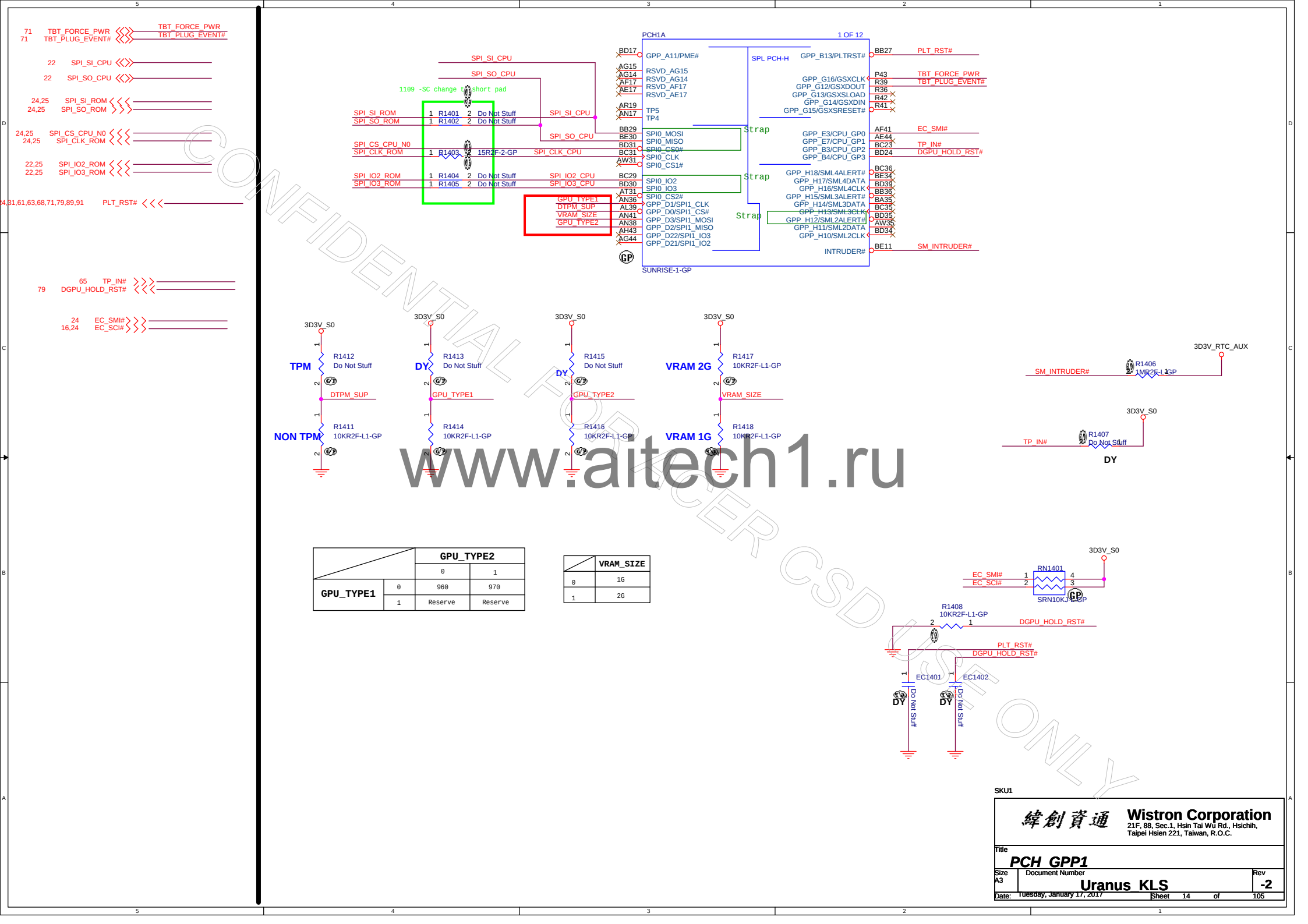
Title: **CPU (Power CAP2)**

Size	Document Number	Rev
A4	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 11 of 105


DM1A
DM1B
DM1C
DM1D
DDR4-260P-17-GP-U
RF RESERVED
FOLLOW CRB
Near DM1.108
-2 20170110
1109 -SC change to short pad
062.10011.00P1
2nd = 062.10011.00K1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR4-SODIMM1
Uranus_KLS
455.0BP01.0001
Tuesday, January 17, 2017
Sheet 12 of 105





GPU_TYPE1 \ GPU_TYPE2	0	1
0	960	970
1	Reserve	Reserve

VRAM_SIZE	
0	1G
1	2G

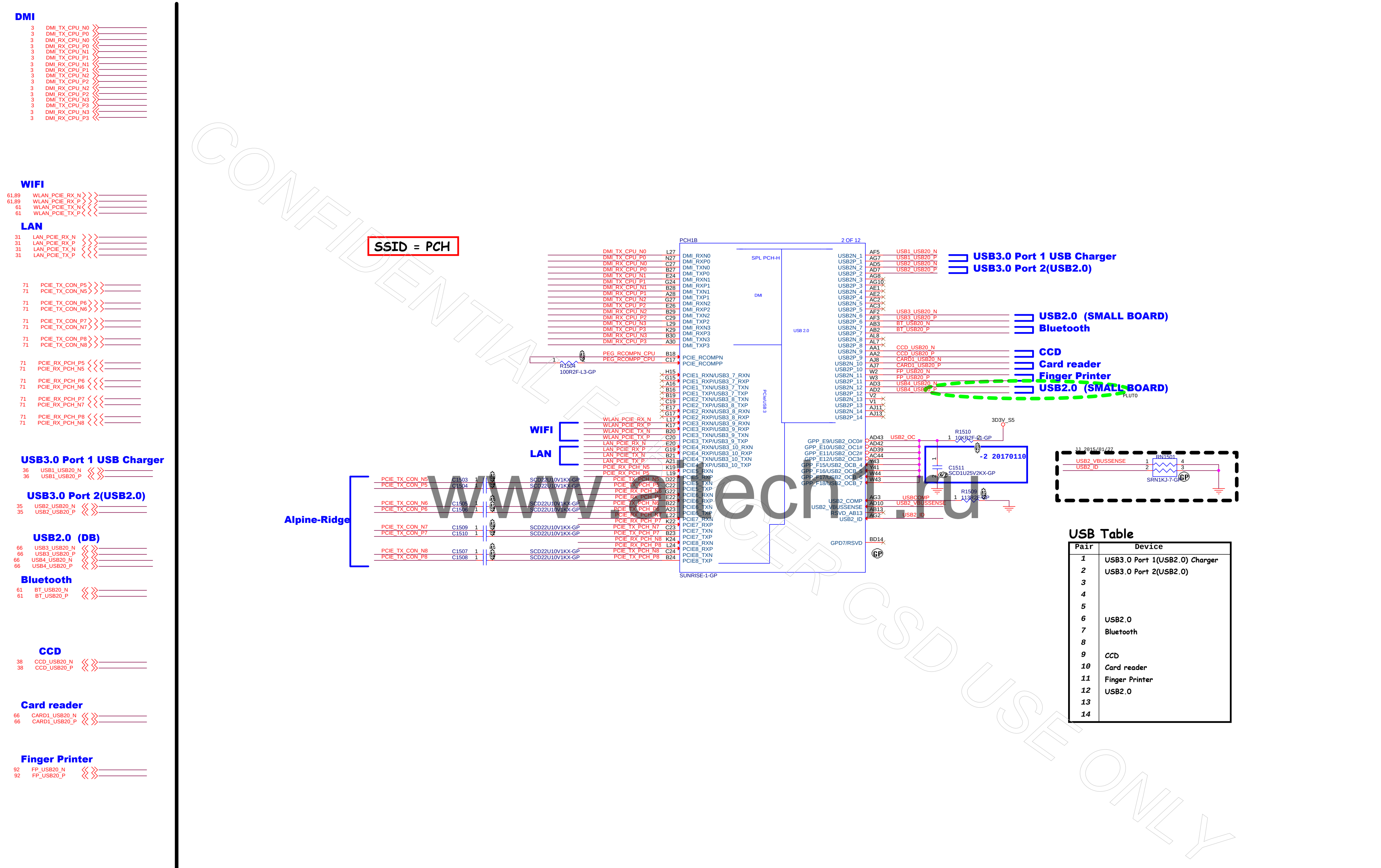
SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH GPP1

Size	Document Number	Rev
A3	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 14 of 105



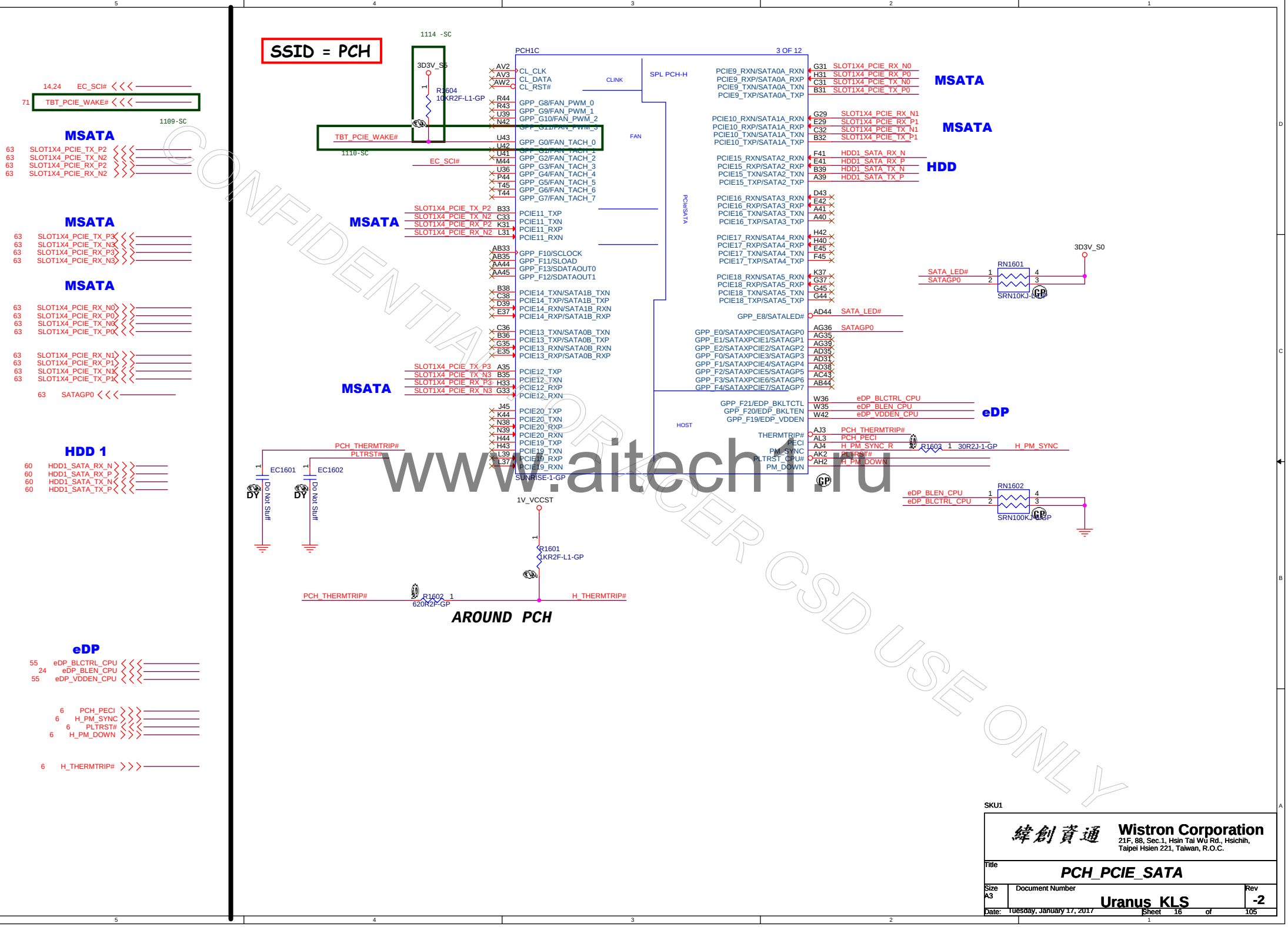
USB Table

Pair	Device
1	USB3.0 Port 1(USB2.0) Charger
2	USB3.0 Port 2(USB2.0)
3	
4	
5	
6	USB2.0
7	Bluetooth
8	
9	CCD
10	Card reader
11	Finger Printer
12	USB2.0
13	
14	

SKU1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_PCIE_DMI_USB
Size: Custom | Document Number: Uranus_KLS | Rev: -2
Date: Tuesday, January 17, 2017 | Sheet 15 of 105



14,24 EC_SCI#
71 TBT_PCIE_WAKE#

MSATA
63 SLOT1X4_PCIE_TX_P2
63 SLOT1X4_PCIE_TX_N2
63 SLOT1X4_PCIE_RX_P2
63 SLOT1X4_PCIE_RX_N2

MSATA
63 SLOT1X4_PCIE_TX_P3
63 SLOT1X4_PCIE_TX_N3
63 SLOT1X4_PCIE_RX_P3
63 SLOT1X4_PCIE_RX_N3

MSATA
63 SLOT1X4_PCIE_RX_N0
63 SLOT1X4_PCIE_RX_P0
63 SLOT1X4_PCIE_TX_N0
63 SLOT1X4_PCIE_TX_P0
63 SLOT1X4_PCIE_RX_N1
63 SLOT1X4_PCIE_RX_P1
63 SLOT1X4_PCIE_TX_N1
63 SLOT1X4_PCIE_TX_P1
63 SATAGP0

HDD 1
60 HDD1_SATA_RX_N
60 HDD1_SATA_RX_P
60 HDD1_SATA_TX_N
60 HDD1_SATA_TX_P

eDP
55 eDP_BLCTRL_CPU
24 eDP_BLEN_CPU
55 eDP_VDDEN_CPU

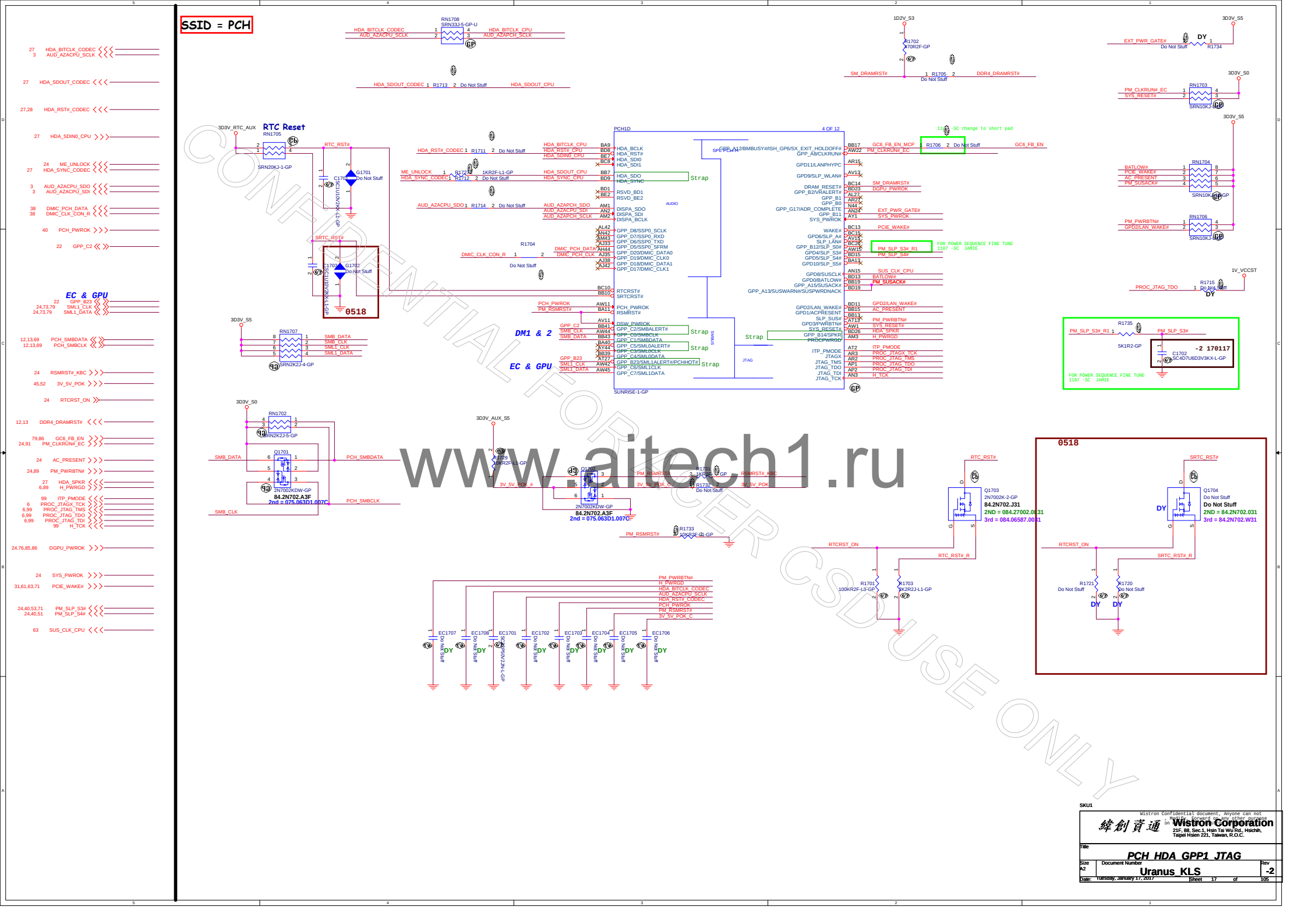
6 PCH_PECI
6 H_PM_SYNC
6 PLTRST#
6 H_PM_DOWN

6 H_THERMTRIP#

SKU1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: PCH_PCIE_SATA		
Size: A3	Document Number: Uranus_KLS	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 16 of 105	

SSID = PCH



SKU1

Wistron Confidential document, Anyone can not Modify, Forward or Any other purpose on

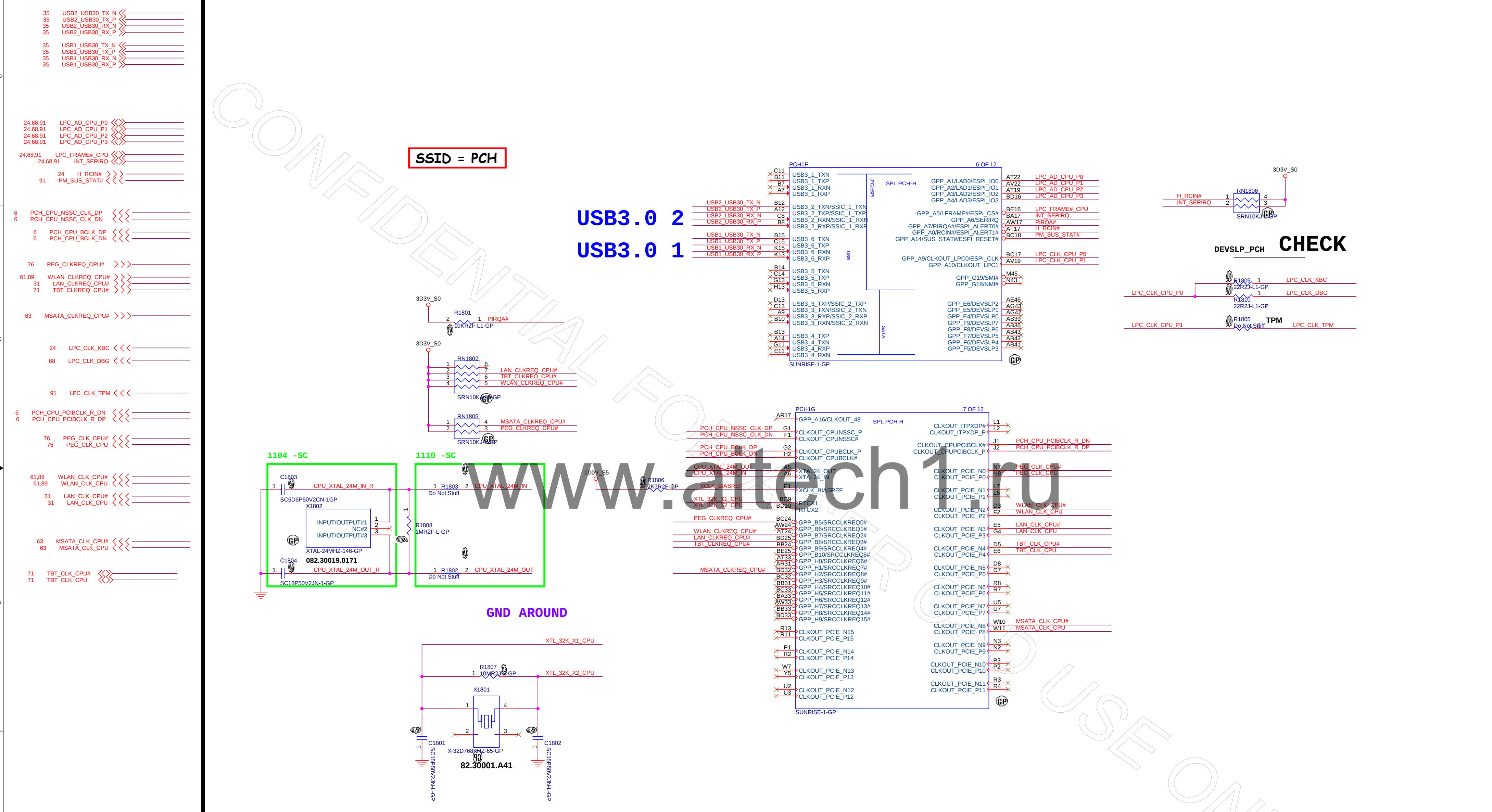
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_HDA_GPP1_JTAG

Size	Document Number	Rev
A2	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 17 of 105



SKU1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH_USB3_CLOCK**

Size: A2 | Document Number: **Uranus_KLS** | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 18 of 105

SSID = PCH

71 DDI1_TBT_HPD_CPU
71 DDI2_TBT_HPD_CPU
71 DDI1_TBT_CLK_CPU
71 DDI1_TBT_DATA_CPU
55 eDP_HPD_CPU
65 KB_BL_DET
22 DDI2_TBT_DATA_CPU
22 DDPD_DATA_CPU
22 GPP_B22/GSPI1_MOSI
86 DGPU_PWR_EN#
25 RTC_DET#
22 GPP_B18/GSPI0_MOSI
79 GPU_EVENT#

TOUCH PAD

65 I2C1_CLK_CPU
65 I2C1_DATA_CPU

69 GSENSOR_INT#
68 LPSS_UART2_TXD
68 LPSS_UART2_RXD
61 WIFI_RF_EN
61,89 BLUETOOTH_EN

PCH1E 5 OF 12
SPL PCH-H
SUNRISE-1-GP

DDI1_TBT_HPD_CPU AW4
DDI2_TBT_HPD_CPU AY2
GPP_I0/DDPB_HPD0
GPP_I1/DDPC_HPD1
GPP_I2/DDPD_HPD2
GPP_I3/DDPE_HPD3
eDP_HPD_CPU BD7
GPP_I4/EDP_HPD

Strap GPP_I7/DDPC_CTRLCLK BB3
GPP_I8/DDPC_CTRLDATA BD6
Strap GPP_I5/DDPB_CTRLCLK BA5
GPP_I6/DDPB_CTRLDATA BC4
Strap GPP_I9/DDPD_CTRLCLK BE5
GPP_I10/DDPD_CTRLDATA BE6

DDI2_TBT_DATA_CPU
DDI1_TBT_CLK_CPU
DDI1_TBT_DATA_CPU
DDPD_DATA_CPU

GPP_F14 Y44 VR_HDMI_DET
GPP_F23 V44 TPM_TYPE
GPP_F22 W39 KB_BL_DET
1110-SC FOR TPM TYPE SELECT
0829 -SB

GPP_G23 L43
GPP_G22 L44
GPP_G21 U35 WIFI_RF_EN
GPP_G20 R35 BLUETOOTH_EN
GPP_H23 BD36

3D3V_S0
PSW_CLR# 1 R1906 2 10KR2F-L1-GP
VR_HDMI_DET 1 R1905 2 DY Do Not Stuff

1 R1904 2 DGPU_PWR_EN# 10KR2F-L1-GP

PSW_CLR#
Pass Word Clear
G1901
Do Not Stuff

3D3V_S5
RN1904 1 2 4 3 RTC_DET# GPU_EVENT# SRN10KJ-L-GP

PCH1K 11 OF 12
SPL PCH-H
SUNRISE-1-GP

GPP_B22/GSPI1_MOSI AT29
DGPU_PWR_EN# AR29
PSW_CLR# AV29
RTC_DET# BC27
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS#

GPP_B18/GSPI0_MOSI BD28
GPU_EVENT# BD27
GPP_B17/GSPI0_MISO AW27
GPP_B16/GSPI0_CLK AR24
GPP_B15/GSPI0_CS#

GPP_C9/UART0_TXD AV44
GPP_C8/UART0_RXD BA41
GPP_C11/UART0_CTS# AU44
GPP_C10/UART0_RTS# AV43

GPP_C15/UART1_CTS#/ISH_UART1_CTS# AU41
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AT44
GPP_C13/UART1_TXD/ISH_UART1_TXD AT43
GPP_C12/UART1_RXD/ISH_UART1_RXD AU43

LPSS_UART2_CTS# AN43
LPSS_UART2_RTS# AN44
LPSS_UART2_TXD AR39
LPSS_UART2_RXD AR45
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD

I2C1_CLK_CPU AR41
I2C1_DATA_CPU AR44
GPP_C19/I2C1_SCL AR38
GPP_C18/I2C1_SDA AT42
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA

GPP_D4/ISH_I2C2_SDA AM44
GPP_D23/ISH_I2C2_SCL AJ44

GPP_D9 AL44
GPP_D10 AL36
GPP_D11 AL35 HDD_Gsensor
GPP_D12 AJ39
1 TP1901

GPP_D16/ISH_UART0_CTS# AJ43
GPP_D15/ISH_UART0_RTS# AL43
GPP_D14/ISH_UART0_TXD AK44
GPP_D13/ISH_UART0_RXD AK45

GPP_H20/ISH_I2C0_SCL BC38
GPP_H19/ISH_I2C0_SDA BB38
GPP_H22/ISH_I2C1_SCL BD38
GPP_H21/ISH_I2C1_SDA BE39

GPP_A23/ISH_GP5 BC22
GPP_A22/ISH_GP4 BD18
GPP_A21/ISH_GP3 BE21
GPP_A20/ISH_GP2 BD22
GPP_A19/ISH_GP1 BD21
GPP_A18/ISH_GP0 BB22 GSENSOR_INT#
GPP_A17/ISH_GP7 BC19

3D3V_S0
RN1901 1 2 4 3 I2C1_DATA_CPU I2C1_CLK_CPU SRN2K2J-L-GP

TOUCH PAD

3D3V_S0
R1903 1 LAB Do Not Stuff LPSS_UART2_CTS#
R1908 1 LAB Do Not Stuff LPSS_UART2_RTS#
R1909 1 LAB Do Not Stuff LPSS_UART2_TXD
R1910 1 LAB Do Not Stuff LPSS_UART2_RXD

3D3V_S0
R1915 Do Not Stuff
TPM2.0
TPM_TYPE
R1916 Do Not Stuff
TPM1.2
1110-SC FOR TPM TYPE SELECT

3D3V_S0
R1914 10KR2F-L1-GP
HDD G sensor
HDD_Gsensor
R1913 10KR2F-L1-GP
Non HDD Gensor

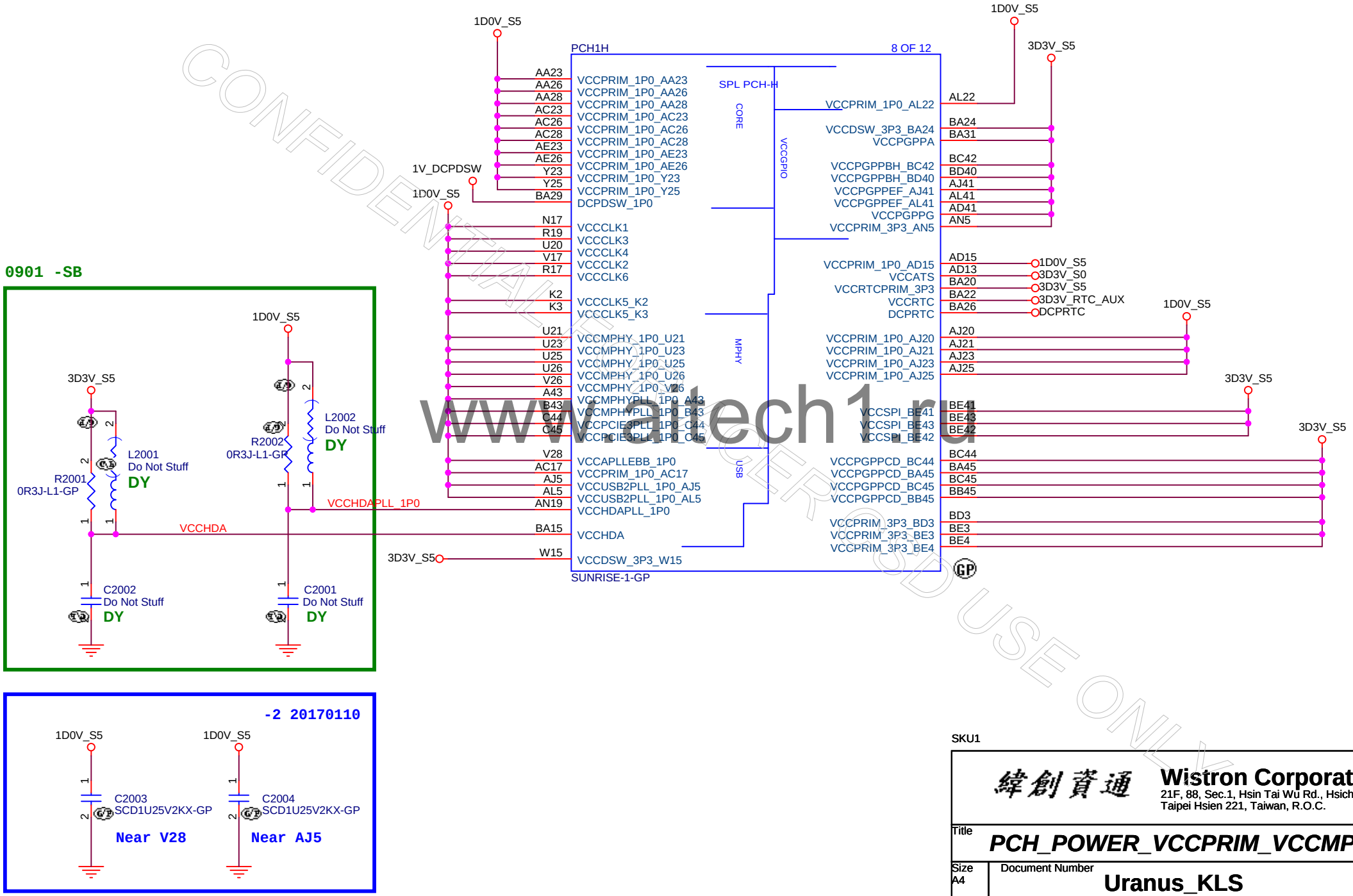
1 Support
0 no support

SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_GPP2_GPP3
Size: A3
Document Number: Uranus_KLS
Rev: -2
Date: Tuesday, January 17, 2017
Sheet 19 of 105

SSID = PCH



0901 -SB

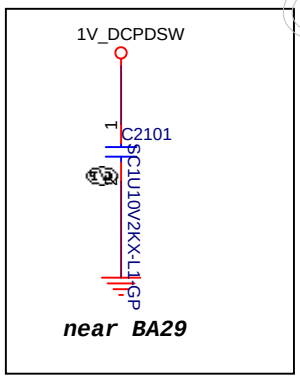
-2 20170110

SKU1

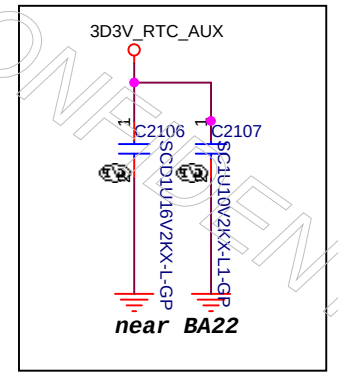
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH_POWER_VCCPRIM_VCCMPHY		
Size: A4	Document Number: Uranus_KLS	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 20 of 105	

SSID = PCH

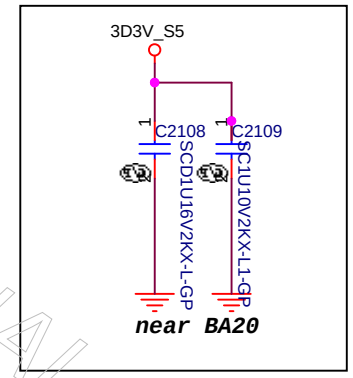
DcpDSW
1x 1uF



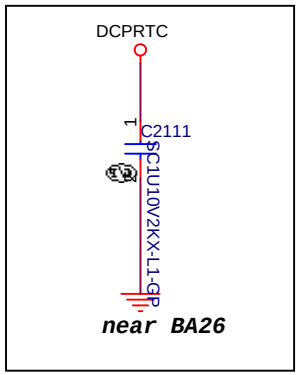
VccRTC
1x1 uF 1x0.1 uF



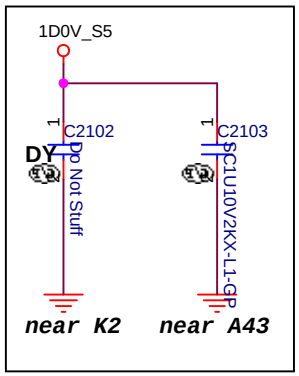
VccRTCPRIM
1x1 uF 1x0.1 uF



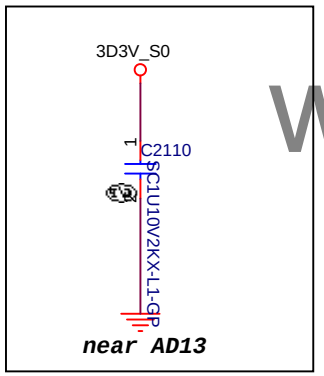
DcpRTC
1x 0.1uF



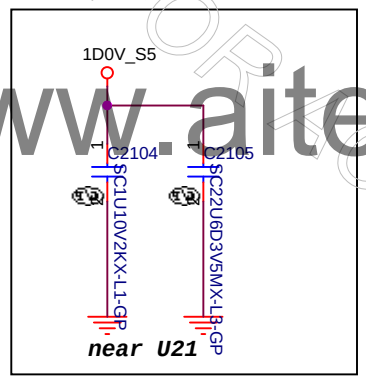
VccMPHYPLL / VccPCIE3PLL
1x1 uF



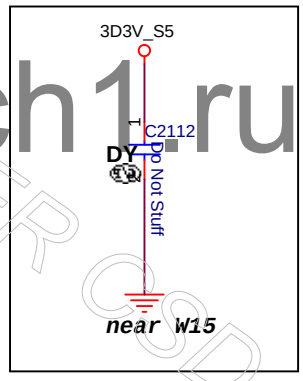
VccATS
1x1 uF



VccMPHY / VccPRIM / VccAPLLEBB
1x1 uF 1x22 uF



VccDSW
1x 1uF



VccPGPPBCH / VccPGPPEF / VccPGPPG / VccPRIM
4x 0.1 uF

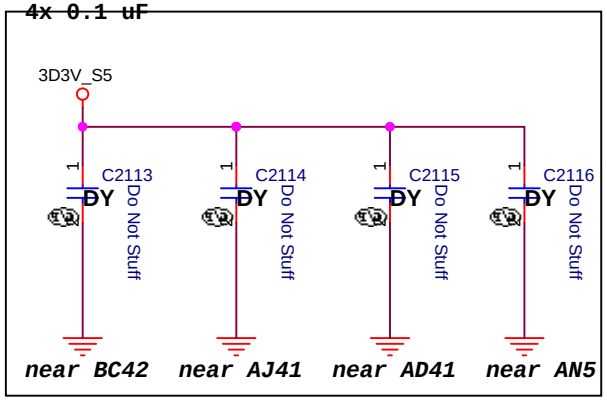


Table 49-8. Decoupling and Power Connection Requirements for KBL H PCH (Sheet 1 of 2)

Voltage Supply	External Pin Name	Ball Number	Edge Cap	Capacitors
V1.0A	VccPRIM_1P0	AJ20, AJ21, AJ23, AJ25, AA23, AA26, AA28, AC23, AC26, AC28, AE23, AE26, Y23, Y25, AL22, AD15		
	VccPRIM_1P0	AC17		
	VccMPHY_1P0	U21, U23, U25, U26, V26	E (<3mm) E (<5mm)	1x 1uF 0402 1x 22uF 0805
	VccAPLLEBB_1P0	V28		
	VccAMPHYPLL_1P0 VccMIPIPLL_1P0	A43, B43 C44, C45	E (<5mm)	1x 1uF 0402
	VccUSB2PLL_1P0, VccHDAPLL_1P0	AJ5, AL5 AN19	Notes	
	VccCLK1, VccCLK2	N17 R17, V17		
	VccCLK3	R19		
	VccCLK4	U20		
	VccCLK5	K2, K3		
V3.3A	VCCRTCPRIM_3P3	BA20	E (<3mm) E (<5mm)	1x 0.1uF 0402 1x 1uF 0402
	VCCPRIM_3p3	BD3, BE3, BE4		
	VCCPRIM_3p3	AN5		
V3.3A/V1.5A/V1.8A	VCCHDA	BA15		
V3.3A/V1.8A	VCCPGPPBCH	BC42, BD40		
	VCCPGPPEF	AJ41, AL41		
	VCCPGPPG	AD41		
	VCCPGPPA	BA31		
	VCCSPI	BE41, BE42, BE43		
	VCCPGPPD	BC44, BA45, BC45, BB45		
V3.3DSW (3.3V)	VCCDSW_3p3	W15		
	VCCDSW_3p3	BA24		
V3.3RTC (3.3V)	VCCRTC	BA22	E (<3mm) E (<5mm	1x 0.1uF 0402 1x 1uF 0402

SKU1

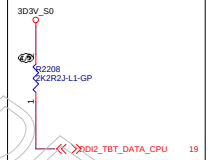
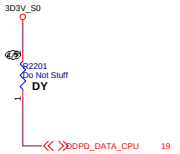
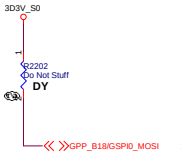
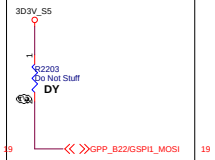
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

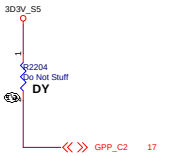
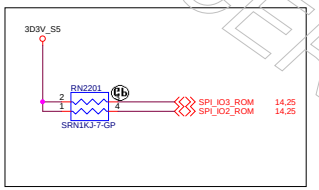
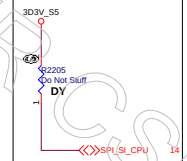
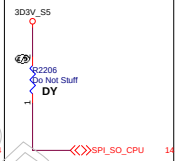
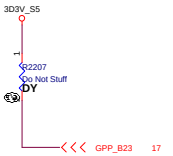
Title: PCH_POWER_CAP1

Size: A4 | Document Number: Uranus_KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 21 of 105

SSID = PCH

Description	Display Port B Detected	Display Port C Detected	Display Port D Detected	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	ESPI FLASH SHARING MODE
GPIO	GPP_I6	GPP_I8	GPP_I10	GPP_B18	GPP_B22	HDA_SDO	GPP_H12
Schematic							
High	Detected	Detected	Detected	Enable	LPC	Disable	1:SLAVE ATTACEHD FLASH SHARING ESPI FLASH SHARING MODE
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	0: MASTER ATTACHED FLASH SHARING
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	eSPI or LPC	TLS Confi-dentiality	Reserved	Reserved	Reserved	Reserved	Reserved
GPIO	GPP_B14	GPP_C5	GPP_C2	SPI0_IO3	SPI0_IO2	SPI0_MOSI	SPI0_MISO	GPP_B23 / PCHHOT#
Schematic							
High	Enable	eSPI	Enable					
Low	Disable	LPC	Disable					
	internal pull-down	internal pull-down	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-down

[H,S,U,Y] Pull-up Resistors on SPI_IO2 and SPI_IO3 Requirement Update

The current Skylake Platform Design Guide (PDG) states that a 1 K pull-up resistor is required on the PCH SPI_IO2 and SPI_IO3 signals.

This 1K pull up resistor is no longer needed on Skylake platforms and can be removed from the motherboard. The new guidelines will be updated in a future release of the Skylake PDG

SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

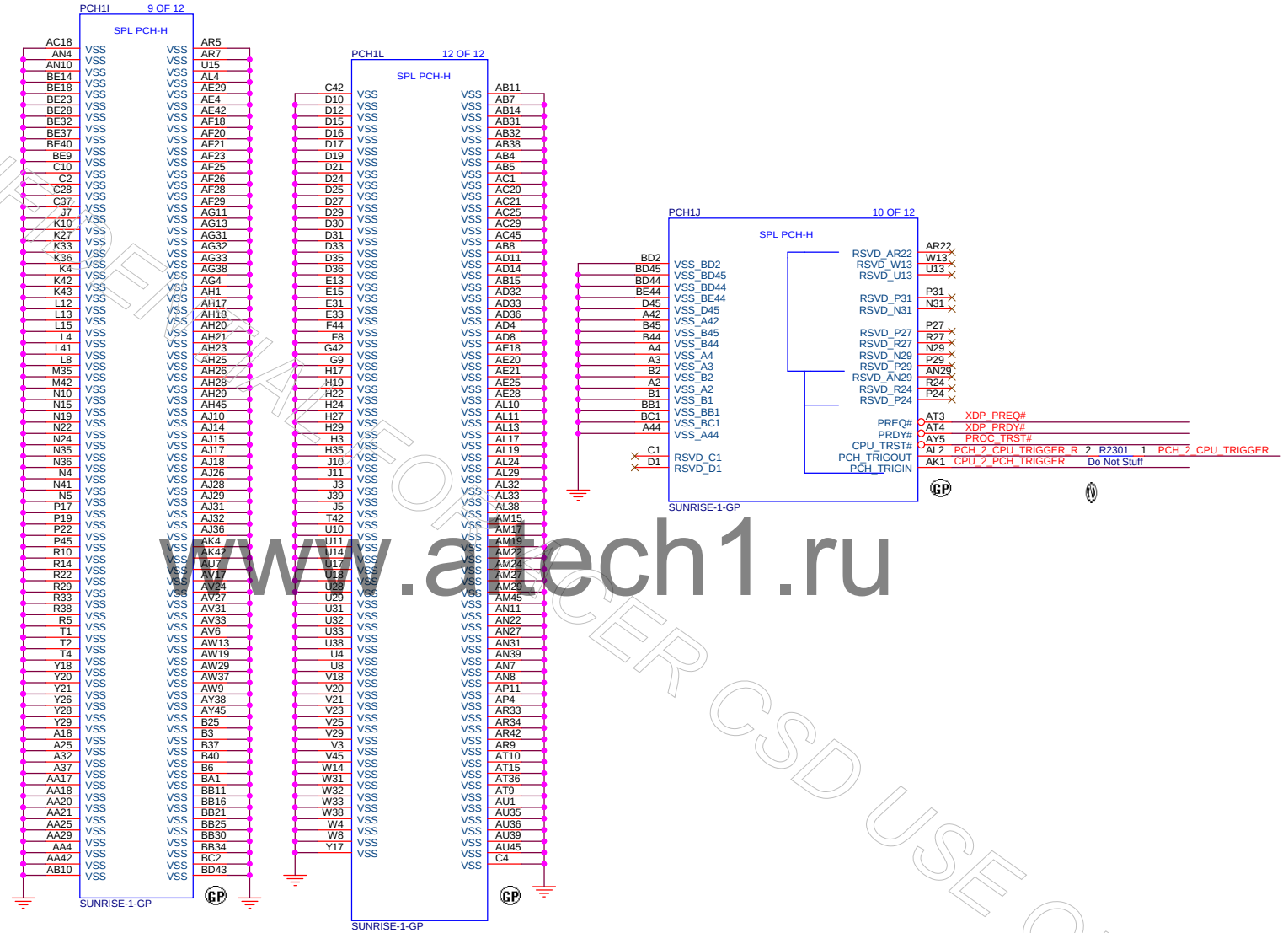
Title: PCH_STRAP

Size: A2 | Document Number: Uranus_KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 22 of 105

6,99 XDP_PREQ#
6,99 XDP_PRDY#
6,99 PROC_TRST#
8 PCH_2_CPU_TRIGGER
8 CPU_2_PCH_TRIGGER

SSID = PCH



SKU1

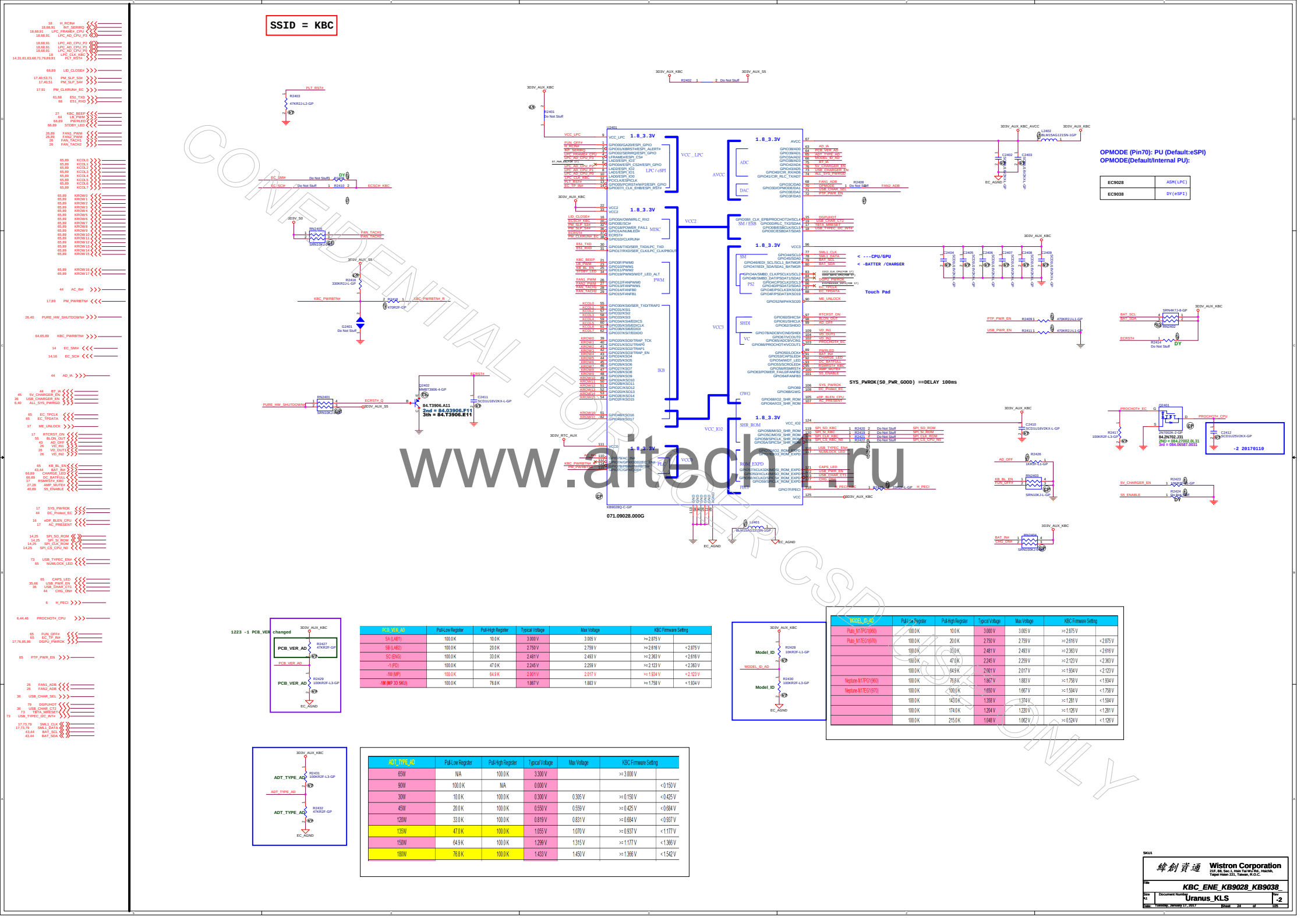
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_RSVD_VSS

Size: A3 | Document Number: Uranus_KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 23 of 105

SSID = KBC



PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA (LAB1)	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
SB (LAB2)	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
SC (ENG)	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
-1 (PD)	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
-1M (MP)	100.0 K	64.9 K	2.017 V	>= 1.934 V	< 2.123 V	
-1M (MP 3D SKU)	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V

Model_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
Pluto_N17P(G1/960)	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
Pluto_N17E(G1/970)	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
	100.0 K	64.9 K	2.017 V	>= 1.934 V	>= 2.123 V	
Neptune-N17P(G1/960)	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
Neptune-N17E(G1/970)	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
	100.0 K	143.0 K	1.368 V	1.374 V	>= 1.261 V	< 1.504 V
	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.261 V
	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.368 V
180W	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.368 V	< 1.542 V

SKU1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

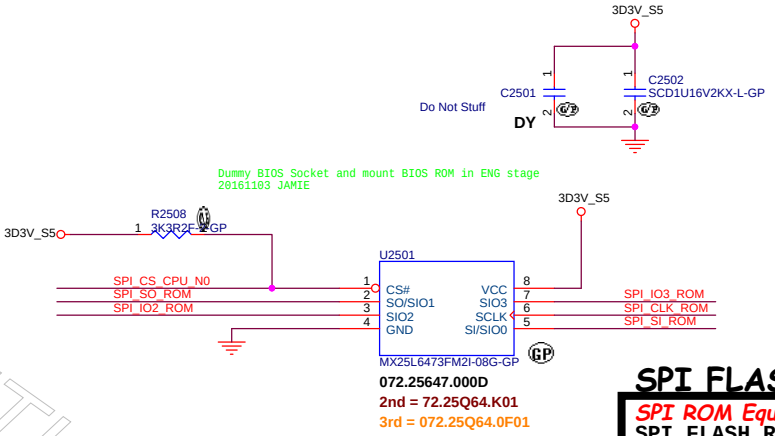
Title: KBC_ENE_KB9028_KB9038_

Size: A1 | Document Number: Uranus_KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 24 of 105

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



14,24 SPI_CS_CPU_N0
14,24 SPI_SO_ROM
14,22 SPI_IO2_ROM
14,22 SPI_IO3_ROM
14,24 SPI_CLK_ROM
14,24 SPI_SI_ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

SPI FLASH ROM (8M byte)

1st= 072.25647.000D (MXIC MX25L6473FM2I-08G)
2nd= 72.25Q64.K01 (WINBOND W25Q64FVSSIQ)
3th= 072.25Q64.0F01 (MICRON N25Q064A13ESED0F)

Main Func = RTC

RTC BATTERY
1st= 023.25212.0011

19 RTC_DET#

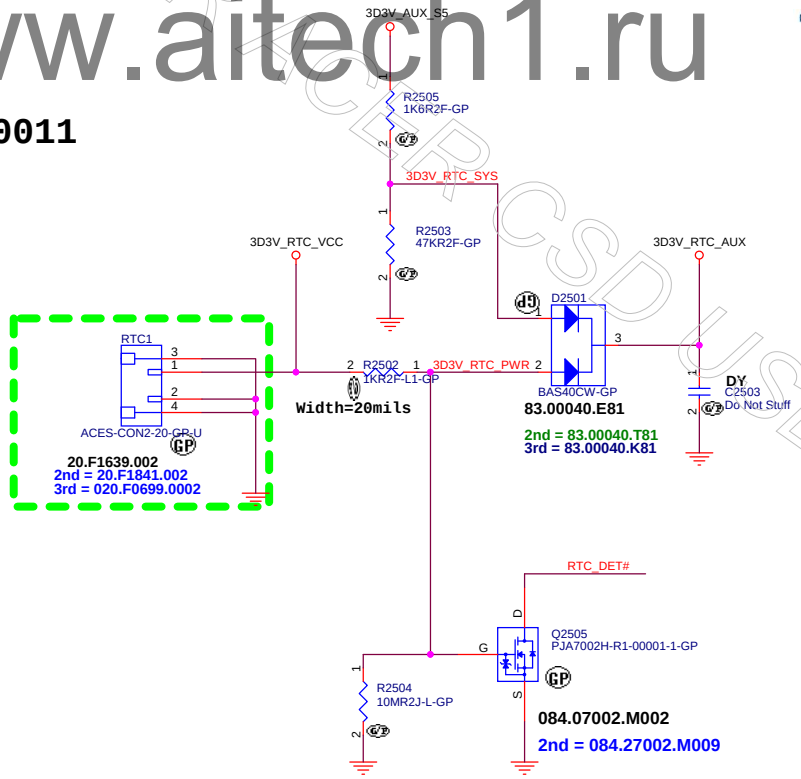
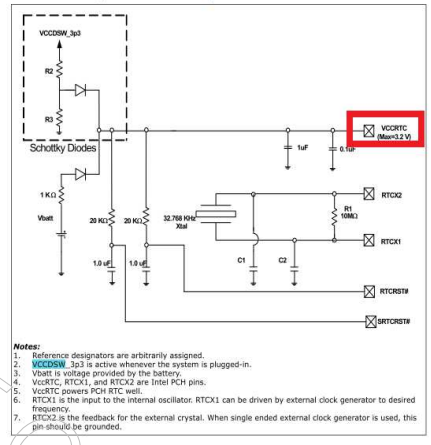


Figure 28-2. External Circuitry for the PCH RTC - Option 1



SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

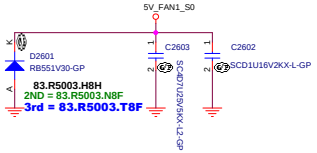
Title: Flash(KBC+PCH)/RTC

Size: A3 | Document Number: Uranus_KLS | Rev: -2

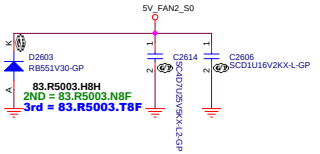
Date: Tuesday, January 17, 2017 | Sheet 25 of 105

SSID = Thermal

Layout 15 mil



Layout 15 mil



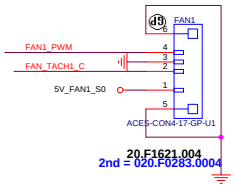
ADB (Active Dusting Blower) function

24 FAN_TACH1
24 FAN_TACH2
24,89 FAN1_PWM
24,89 FAN2_PWM
24 VD_IN1
24 VD_IN2
24 FAN1_ADB
24 FAN2_ADB
24 VD_OUT1
24,40 PURE_HW_SHUTDOWN#
40 IMVP_PWRGD_R

AFTP TESTPOINT

83.R5003.H8H
2ND = 83.R5003.N8F
3rd = 83.R5003.T8F

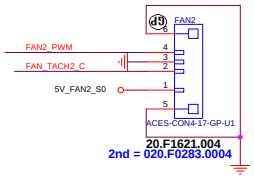
PIN define confirm



20.F1621.004
2nd = 020.F0283.0004

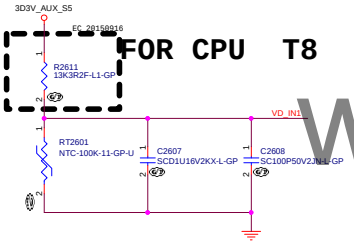
83.R5003.H8H
2ND = 83.R5003.N8F
3rd = 83.R5003.T8F

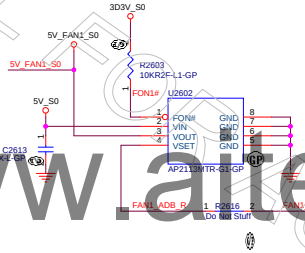
PIN define confirm

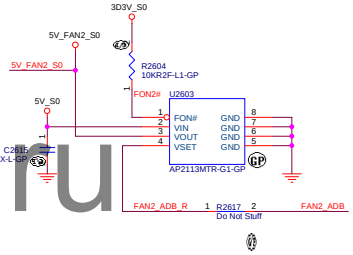


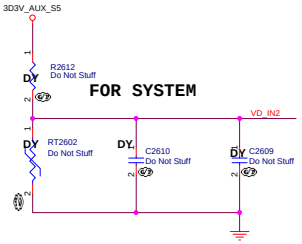
20.F1621.004
2nd = 020.F0283.0004

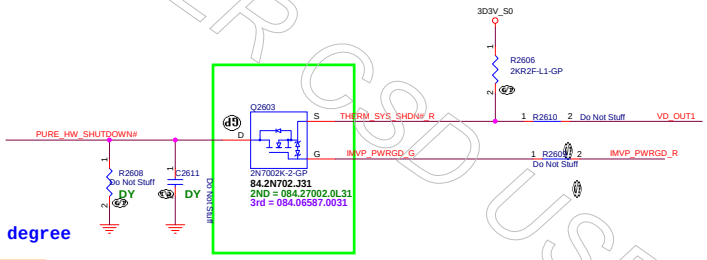
FOR CPU T8





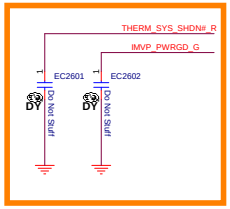






T8 = 85 degree

EMI Reserved



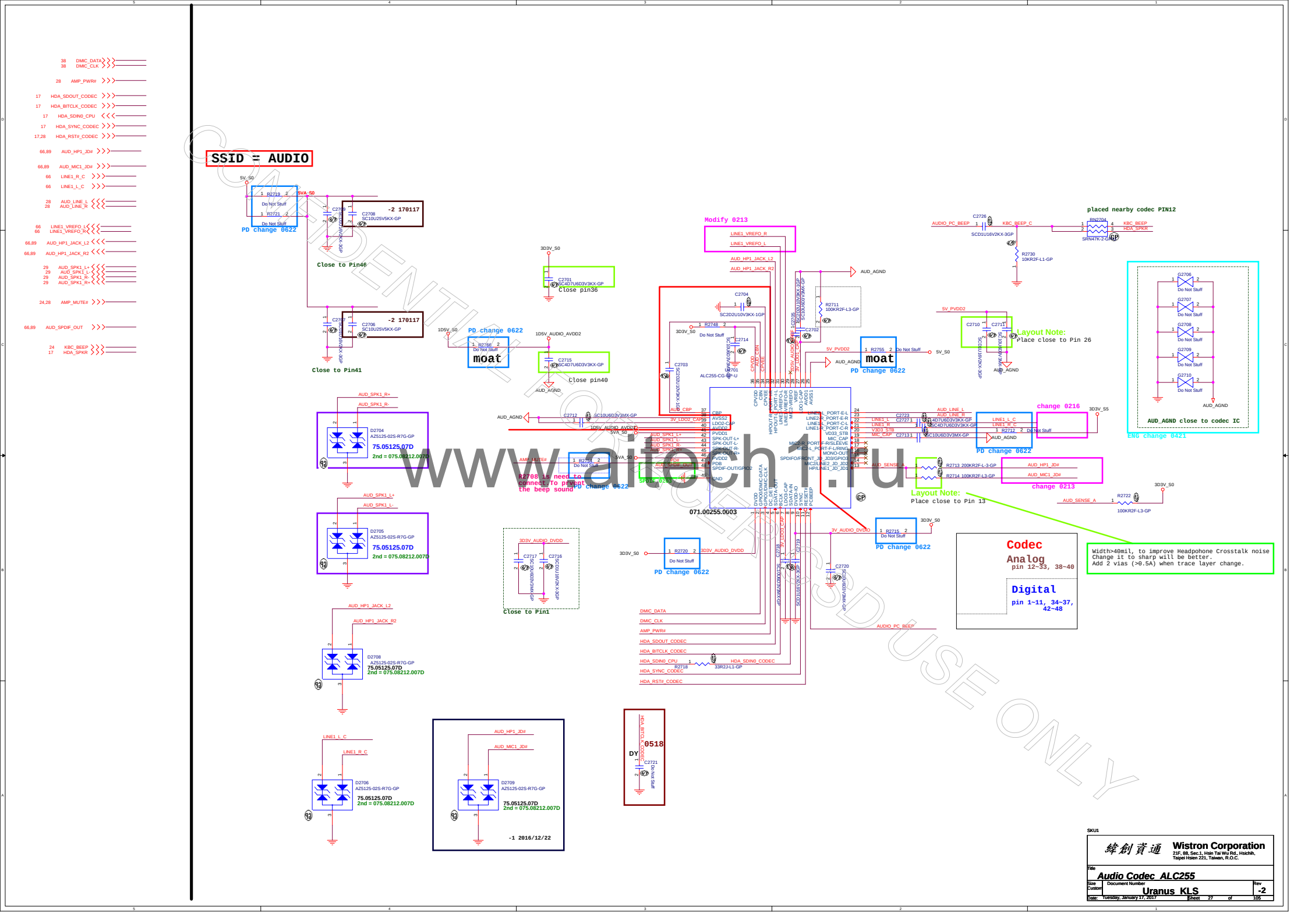
SKU1

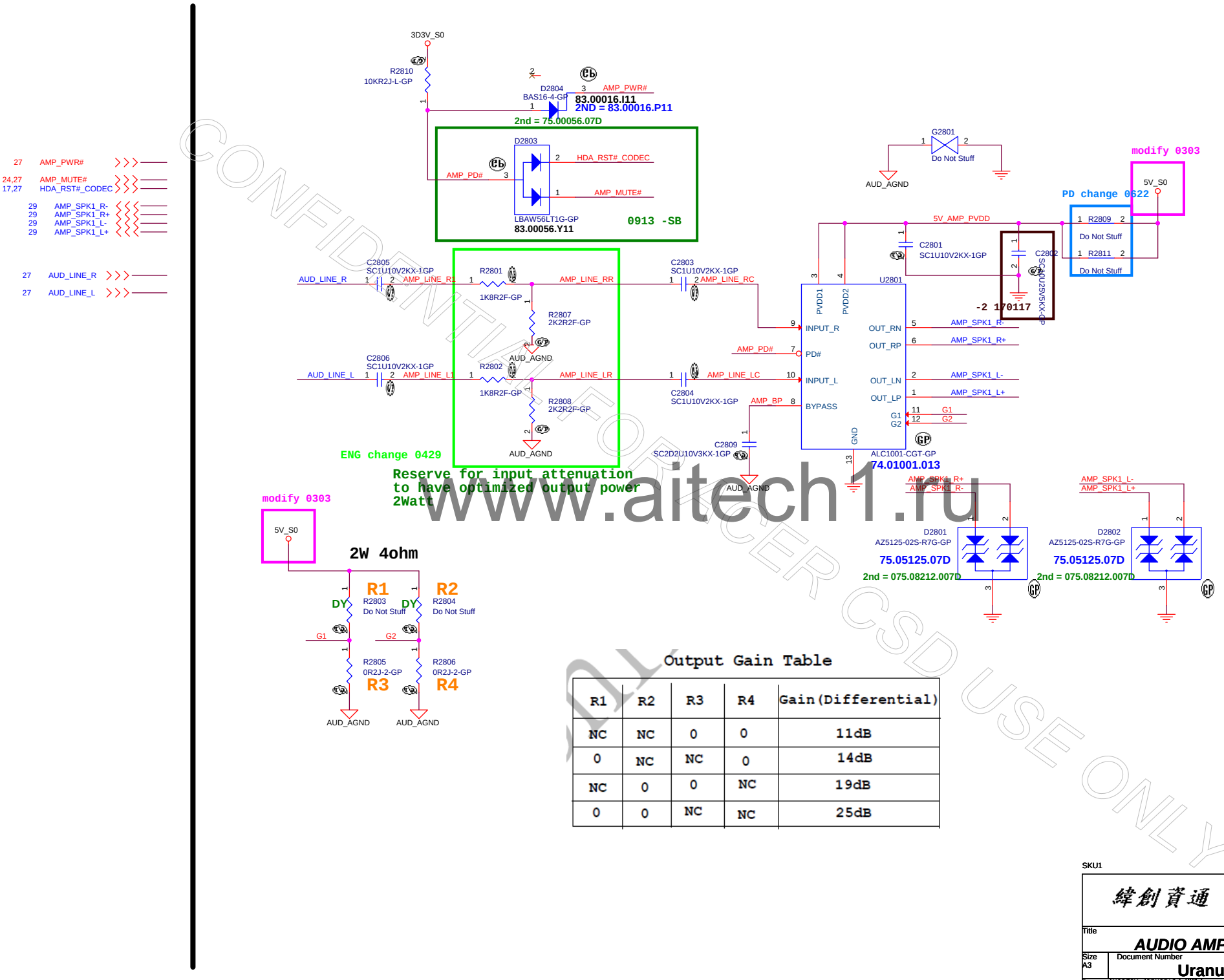
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal T8 and FAN

Size: A2 | Document Number: Uranus_KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 26 of 105


SSID = AUDIO
Modify 0213
placed nearby codec PIN12
Layout Note:
Place close to Pin 26
AUD_AGND close to codec IC
ENG change 0421
change 0216
change 0213
PD change 0622
Close to Pin46
Close to Pin41
Close pin36
Close pin40
Close to Pin1
R2708 is need to connect,To prevent the beep sound
Layout Note:
Place close to Pin 13
Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.
Codec
Analog
pin 12~33, 38~40
Digital
pin 1~11, 34~37, 42~48
071.00255.0003
Wistron Corporation
Audio Codec ALC255
Uranus_KLS
-2
Tuesday, January 17, 2017
Sheet 27 of 105



Output Gain Table

R1	R2	R3	R4	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP ALC1001

Size	Document Number	Rev
A3	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 28 of 105

SSID = AUDIO

Speaker

1110 -SC short pad for EMI suggest

AMP_SPK1_L-	ER2901	1	2	Do Not Stuff	AMP_SPK1_R_L-
AMP_SPK1_L+	ER2902	1	2	Do Not Stuff	AMP_SPK1_R_L+
AUD_SPK1_L-	ER2904	1	2	Do Not Stuff	AUD_SPK1_R_L-
AUD_SPK1_L+	ER2903	1	2	Do Not Stuff	AUD_SPK1_R_L+
AMP_SPK1_R-	ER2906	1	2	Do Not Stuff	AMP_SPK1_R_R-
AMP_SPK1_R+	ER2905	1	2	Do Not Stuff	AMP_SPK1_R_R+
AUD_SPK1_R-	ER2907	1	2	Do Not Stuff	AUD_SPK1_R_R-
AUD_SPK1_R+	ER2908	1	2	Do Not Stuff	AUD_SPK1_R_R+

Layout Note:
Trace width=40mil

EC2906 EC2905 EC2904 EC2903 EC2916 EC2917 EC2918 EC2919
DY Do Not Stuff

SPK1
10 8 7 6 5 4 3 2 1 9
ACES-CON8-12-GP-U2
20.F0818.008

28 AMP_SPK1_L-
28 AMP_SPK1_L+
27 AUD_SPK1_L-
27 AUD_SPK1_L+
28 AMP_SPK1_R-
28 AMP_SPK1_R+
27 AUD_SPK1_R-
27 AUD_SPK1_R+

AFTP TESTPOINT

89 AMP_SPK1_R_L-
89 AMP_SPK1_R_L+
89 AUD_SPK1_R_L-
89 AUD_SPK1_R_L+
89 AMP_SPK1_R_R-
89 AMP_SPK1_R_R+
89 AUD_SPK1_R_R-
89 AUD_SPK1_R_R+

SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/ALC255
Size: A4 | Document Number: Uranus_KLS | Rev: -2
Date: Tuesday, January 17, 2017 | Sheet 29 of 105

SKU1

緯創資通

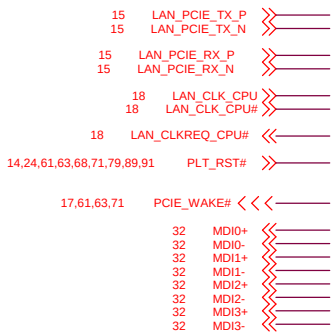
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

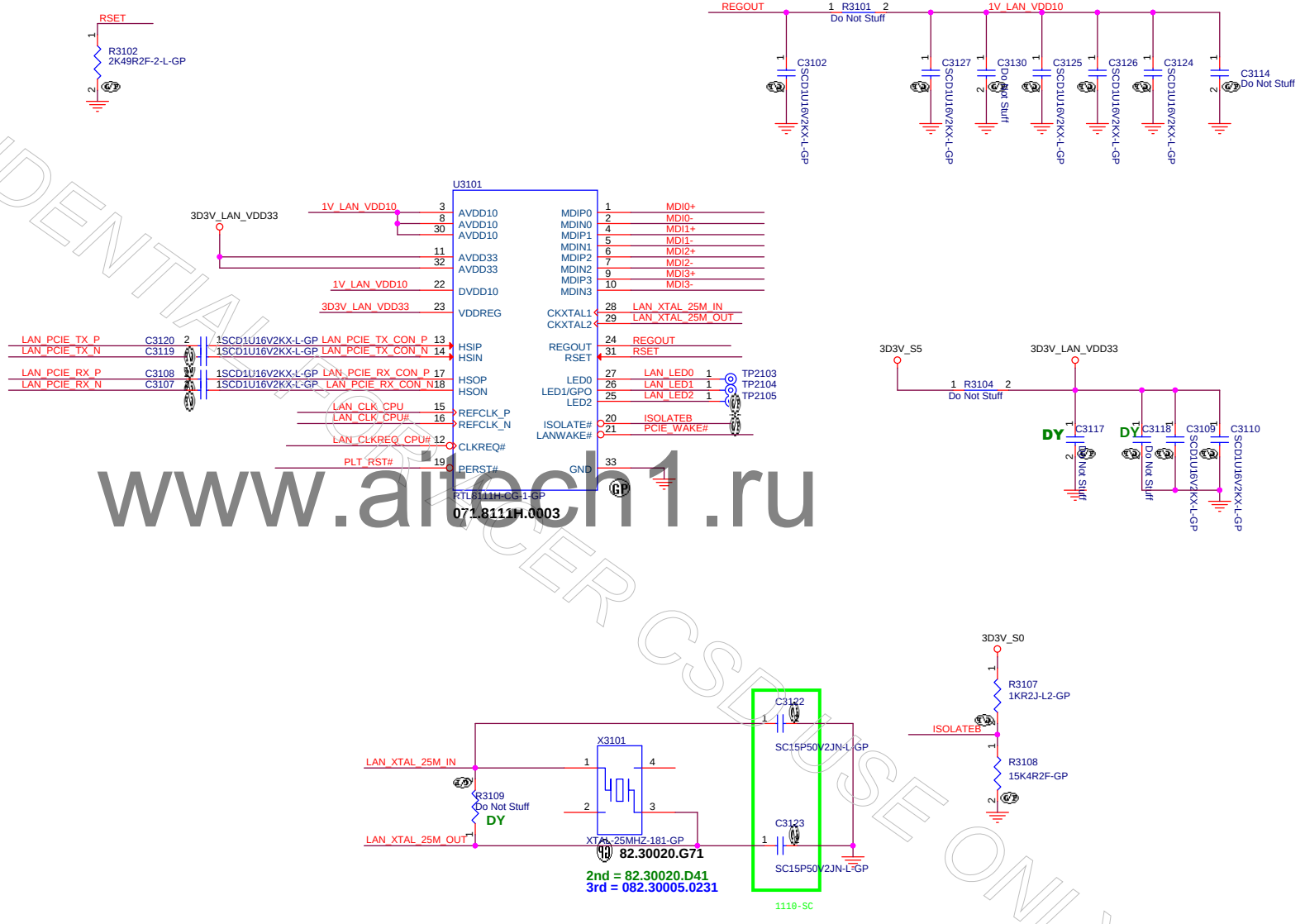
Title

(Reserved)

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 30 of 105





SKU1

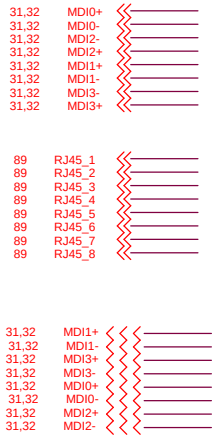
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

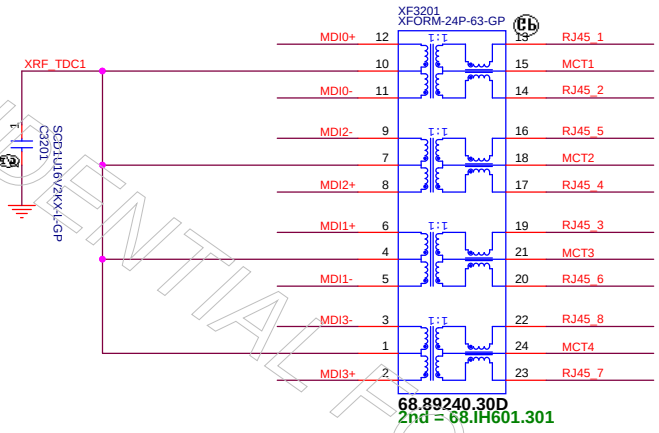
Title: **LAN(RTL8111)**

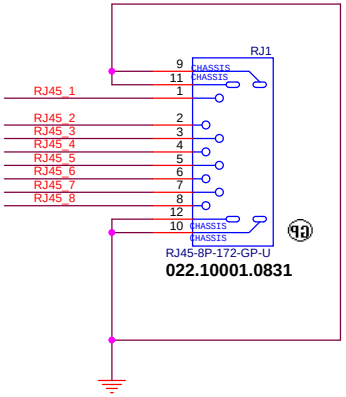
Size	Document Number	Rev
A3	Uranus_KLS	-2

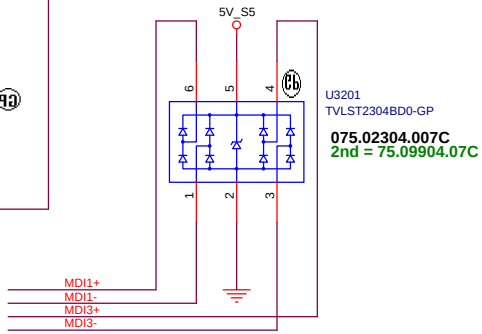
Date: Tuesday, January 17, 2017 Sheet 31 of 105

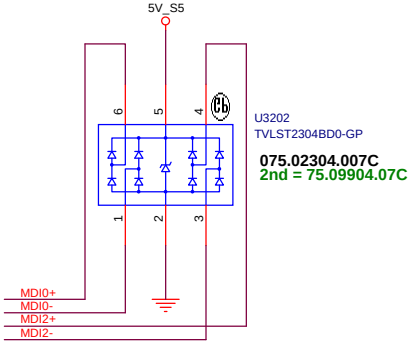
SSID = LAN

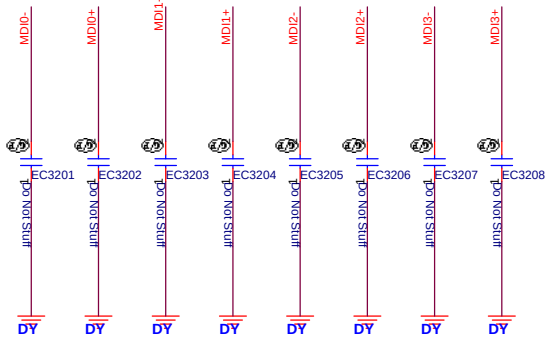


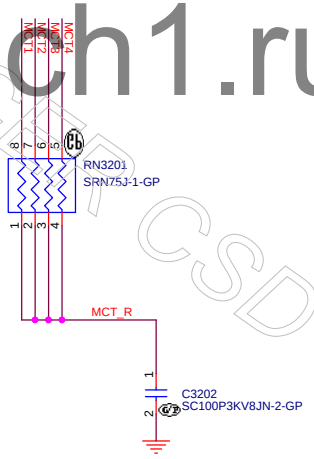












SKU1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *RJ45+Transformer*

Size	Document Number	Rev
A3	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 32 of 105

SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 33 of 105

SKU1

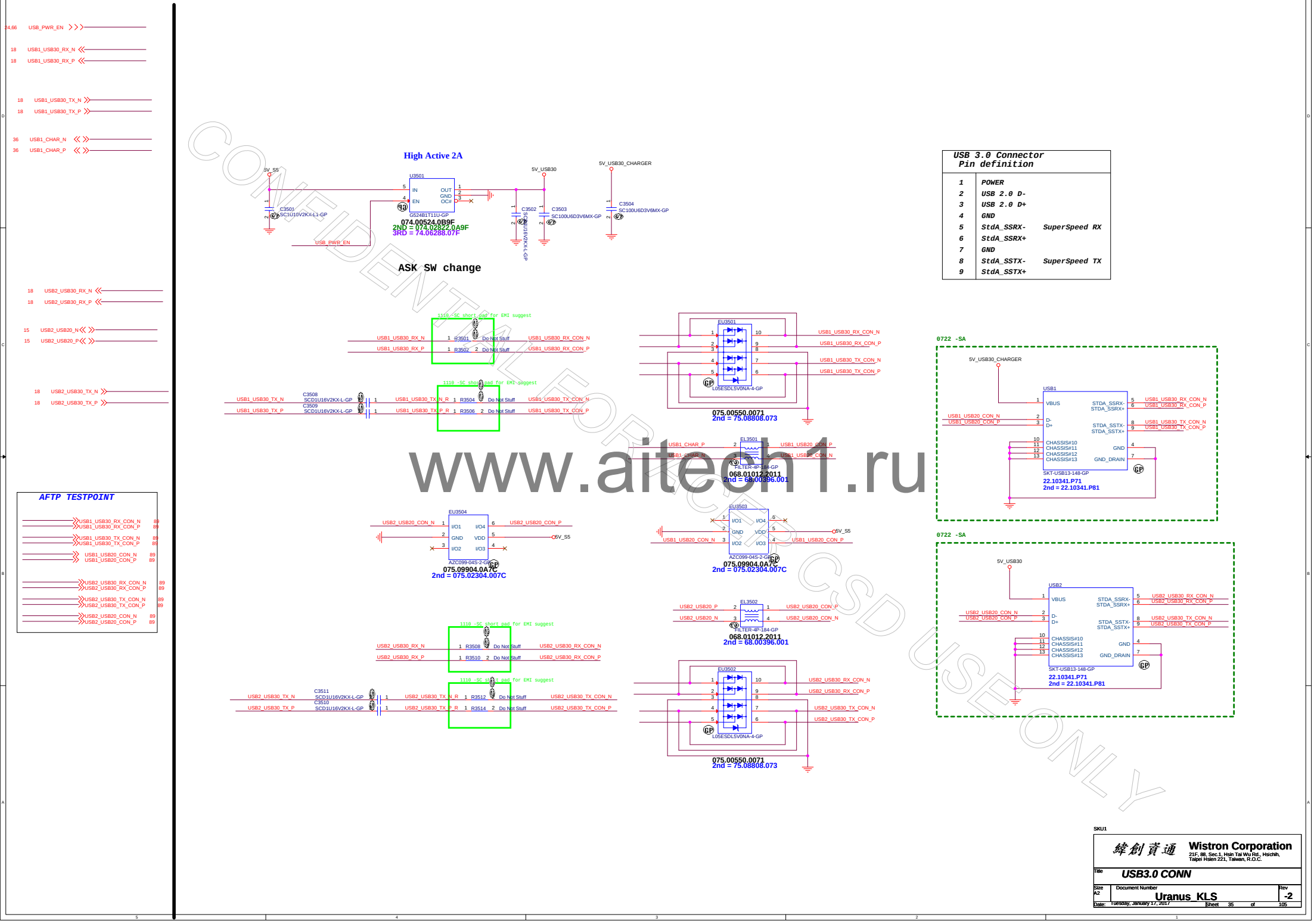
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU_CFG_CFG STRAP

Size	Document Number	Rev
A	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 34 of 105



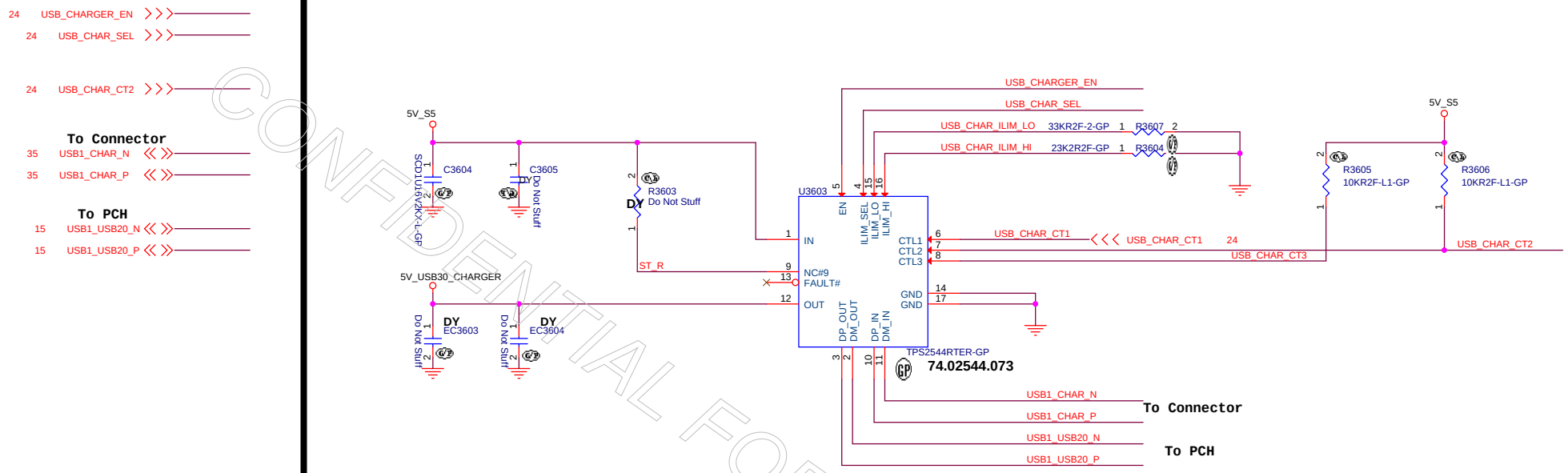


Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_ SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Charging mode
1	0	1	0	DCP/Divider1	ILIM_LO	OFF	Device forced to stay in DCP divider1
1	0	1	1	DCP/Divider1	ILIM_HI	OFF	Charging mode
1	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2	ILIM_LO	OFF	
1	1	1	1	CDP	ILIM_HI	CDP	Data lines disconnected Load Detect function active

SKU1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB CHARGER

Size: A3 | Document Number: Uranus_KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 36 of 105

SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 37 of 105

17 DMIC_CLK_CON_R

17 DMIC_PCH_DATA

27 DMIC_CLK

27 DMIC_DATA

15 CCD_USB20_P

15 CCD_USB20_N

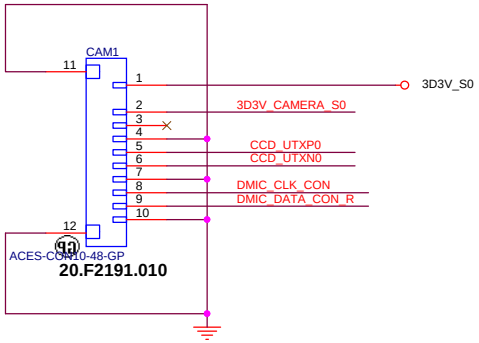
AFTP TESTPOINT

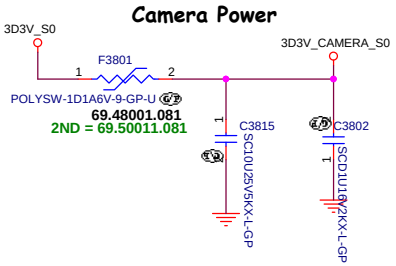
CCD_UTXN0 89

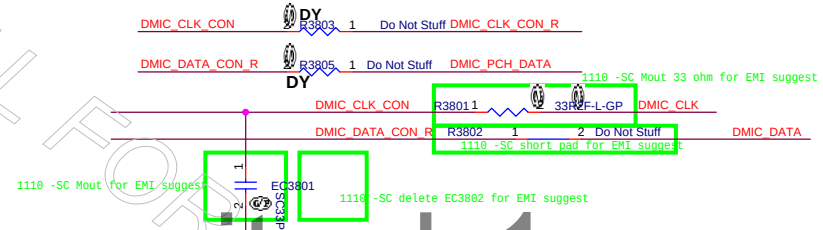
CCD_UTXP0 89

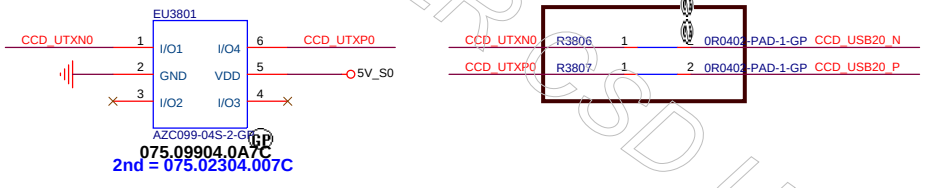
DMIC_CLK_CON 89

DMIC_DATA_CON_R 89









SKU1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB RE_DRIVER_3D CAMERA**

Size	Document Number	Rev
A3	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 38 of 105

SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

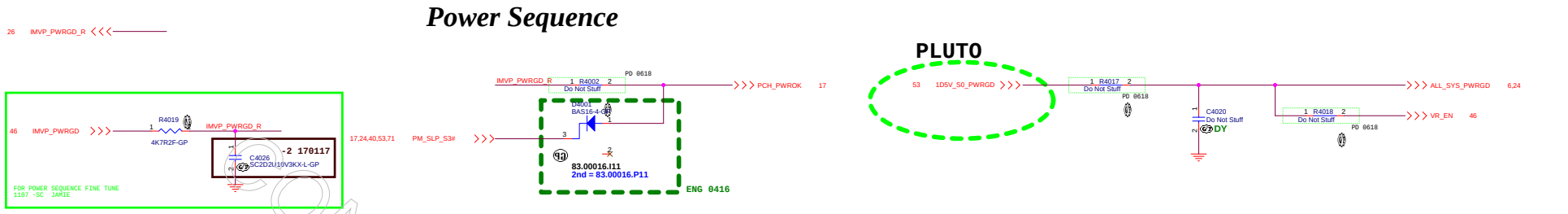
Title

(Reserved)

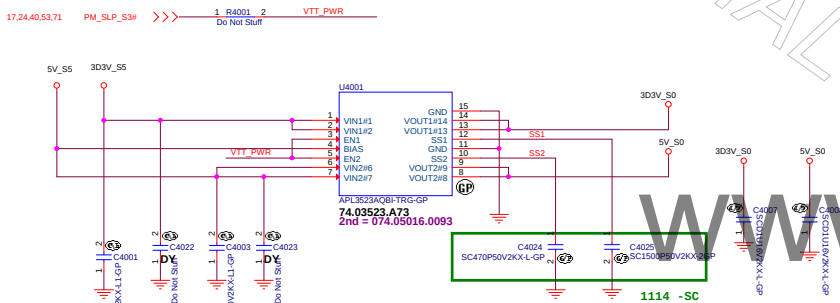
Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

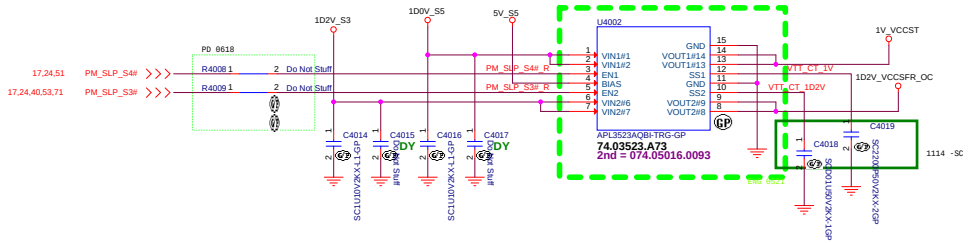
Date: Tuesday, January 17, 2017 Sheet 39 of 105

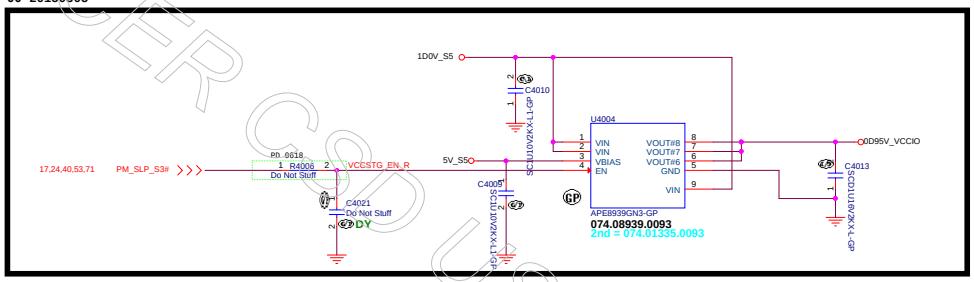
Power Sequence

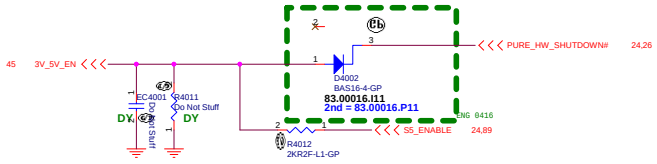


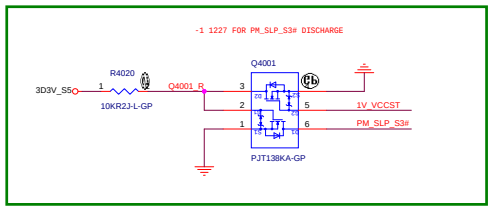
ANNIE Run Power











SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size	Document Number	Rev
A2	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 40 of 105

SKU1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)DS3***

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**
Date: Tuesday, January 17, 2017	Sheet 41 of 105	

SKU1

緯創資通

Wistron Corporation

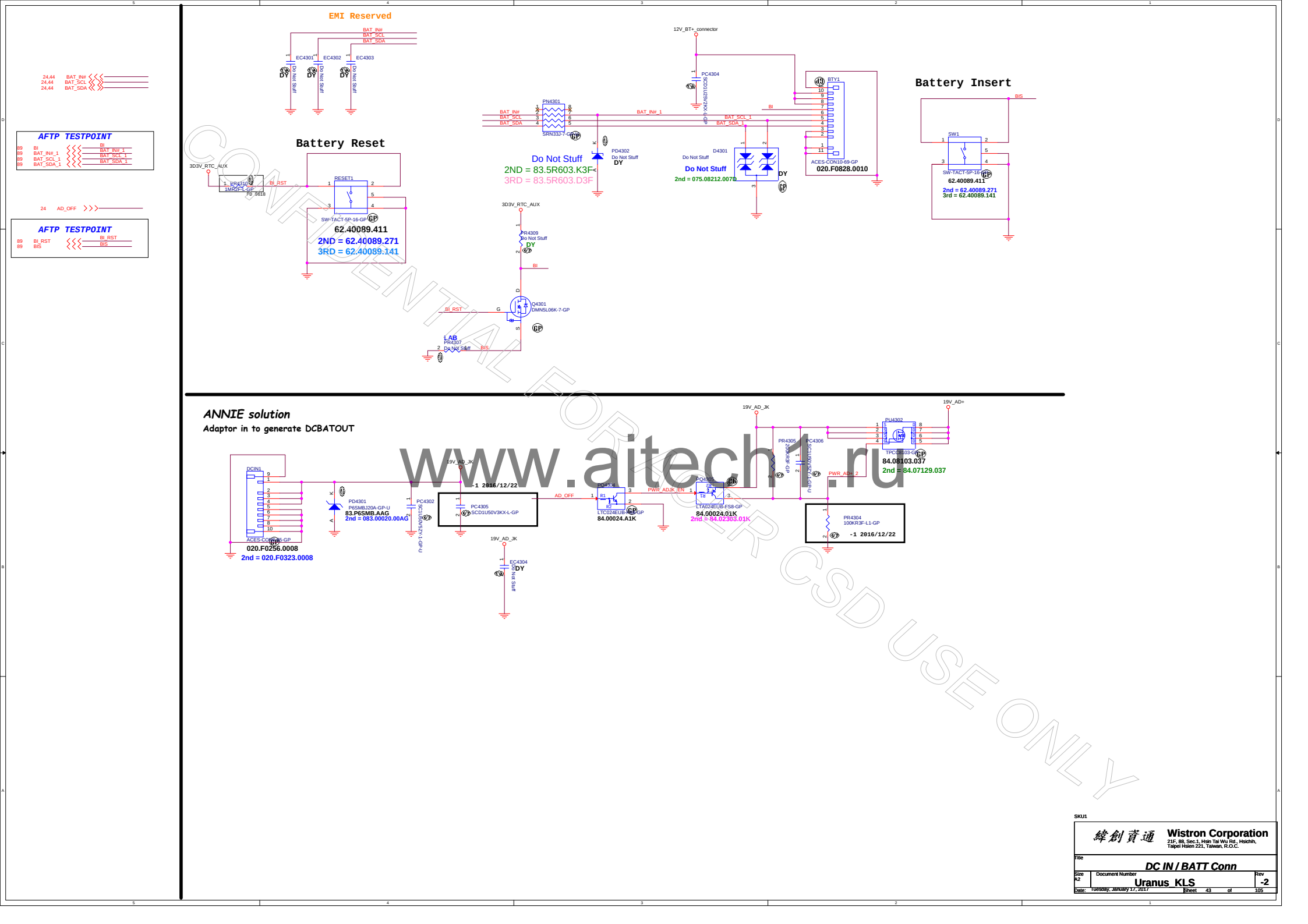
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

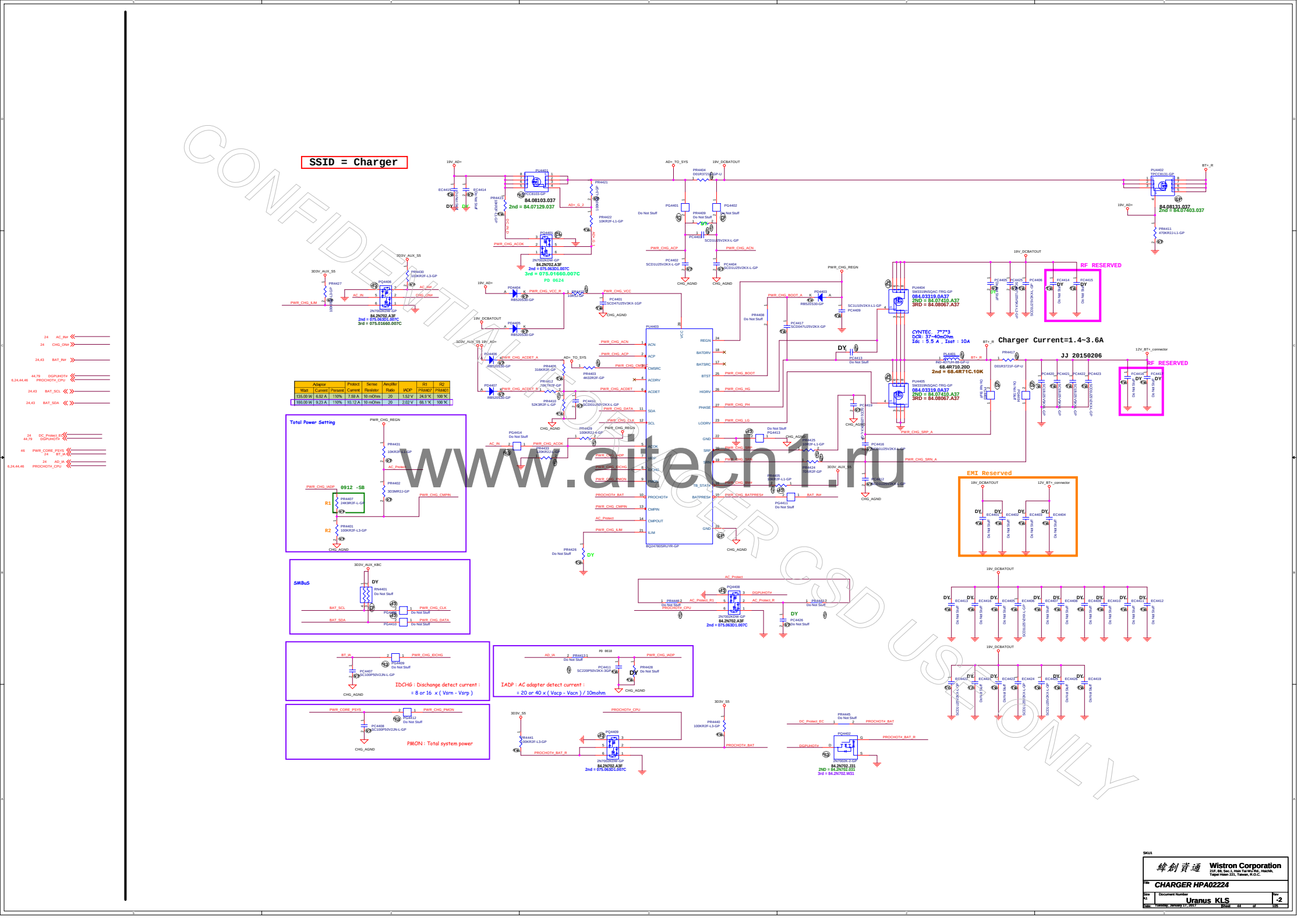
Title

(Reserved)

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 42 of 105





SKU1

蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., HsiChih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER HPA02224

Size: A1 | Document Number: Uranus KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 44 of 105

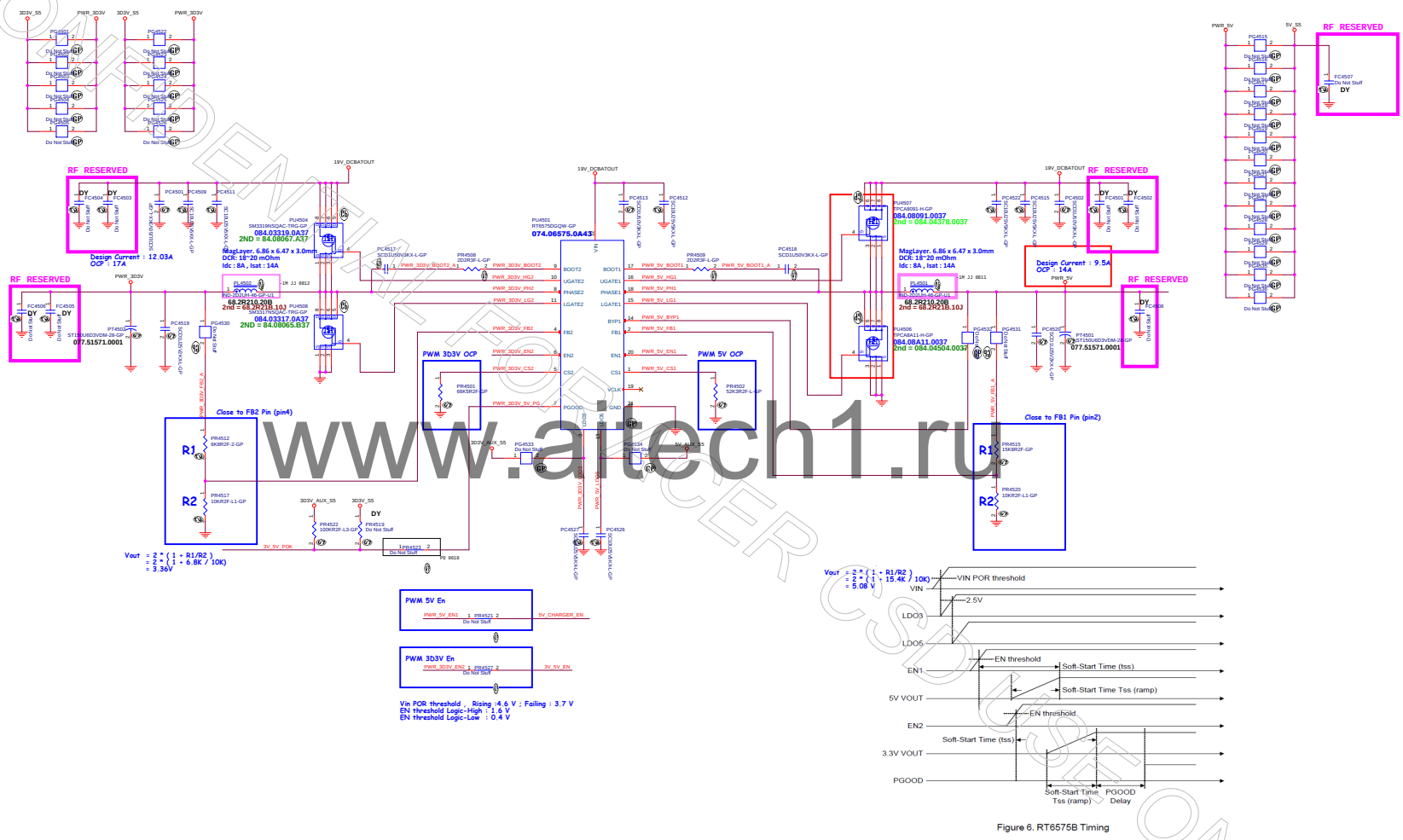
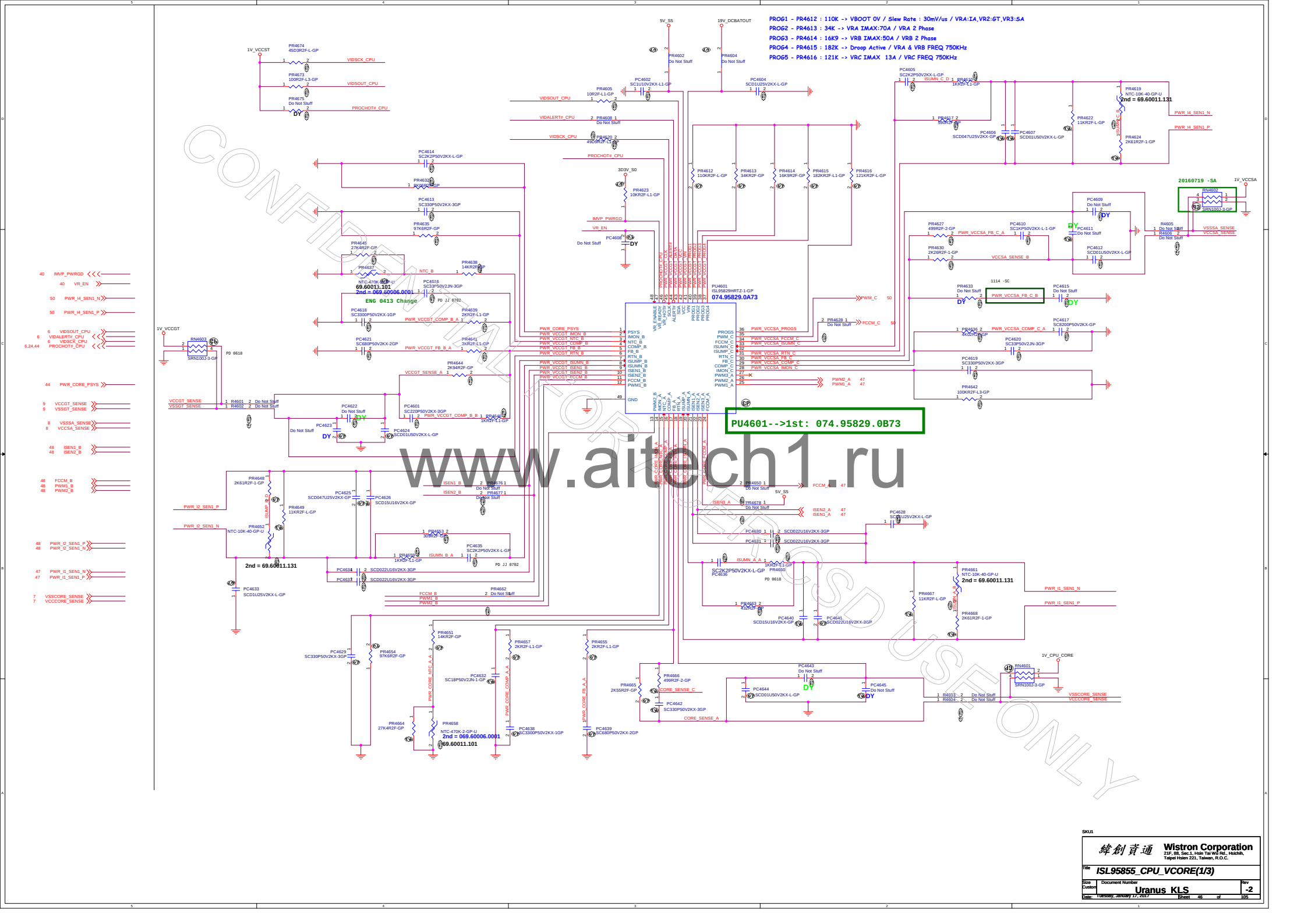
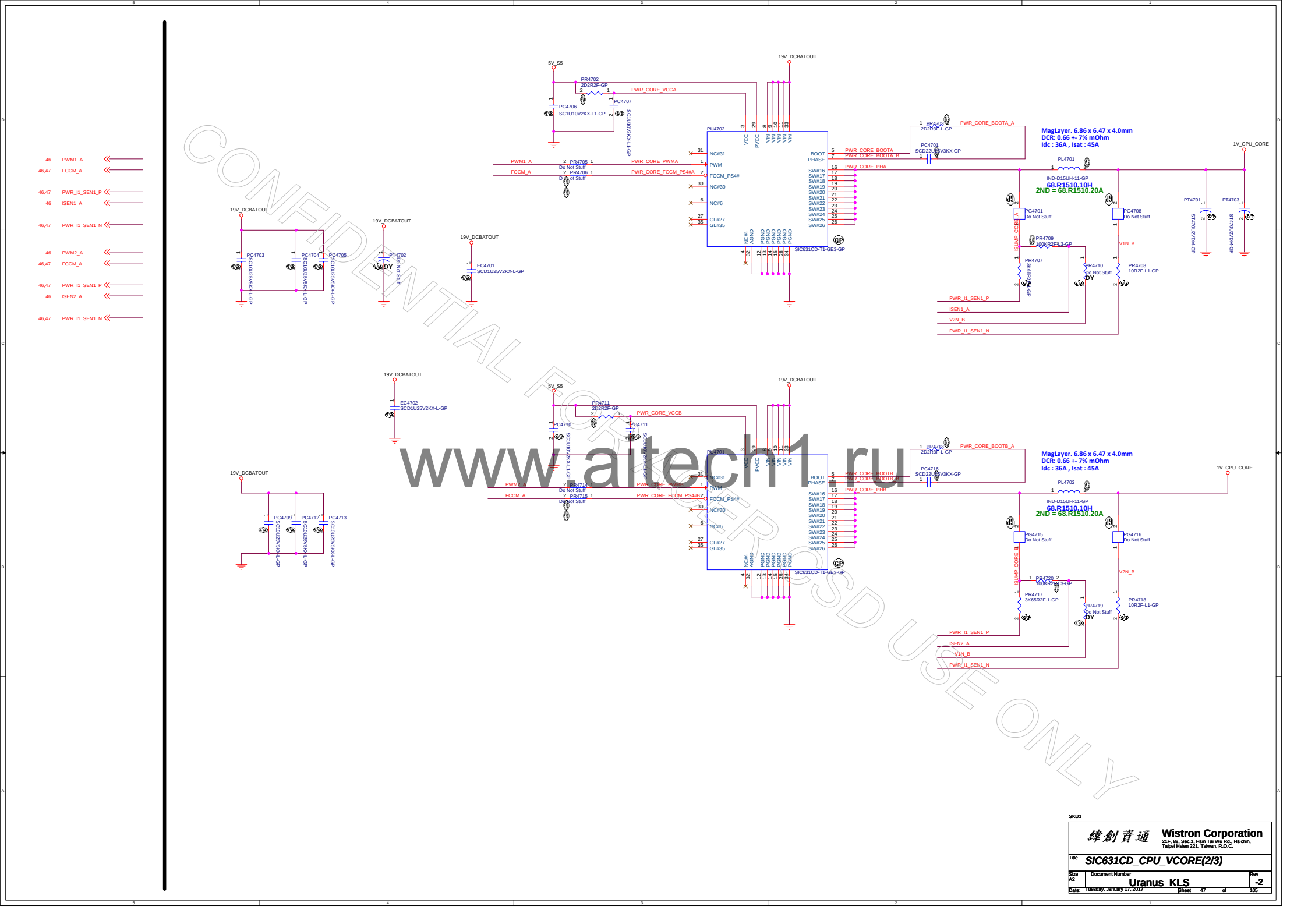


Figure 6. RT6575B Timing

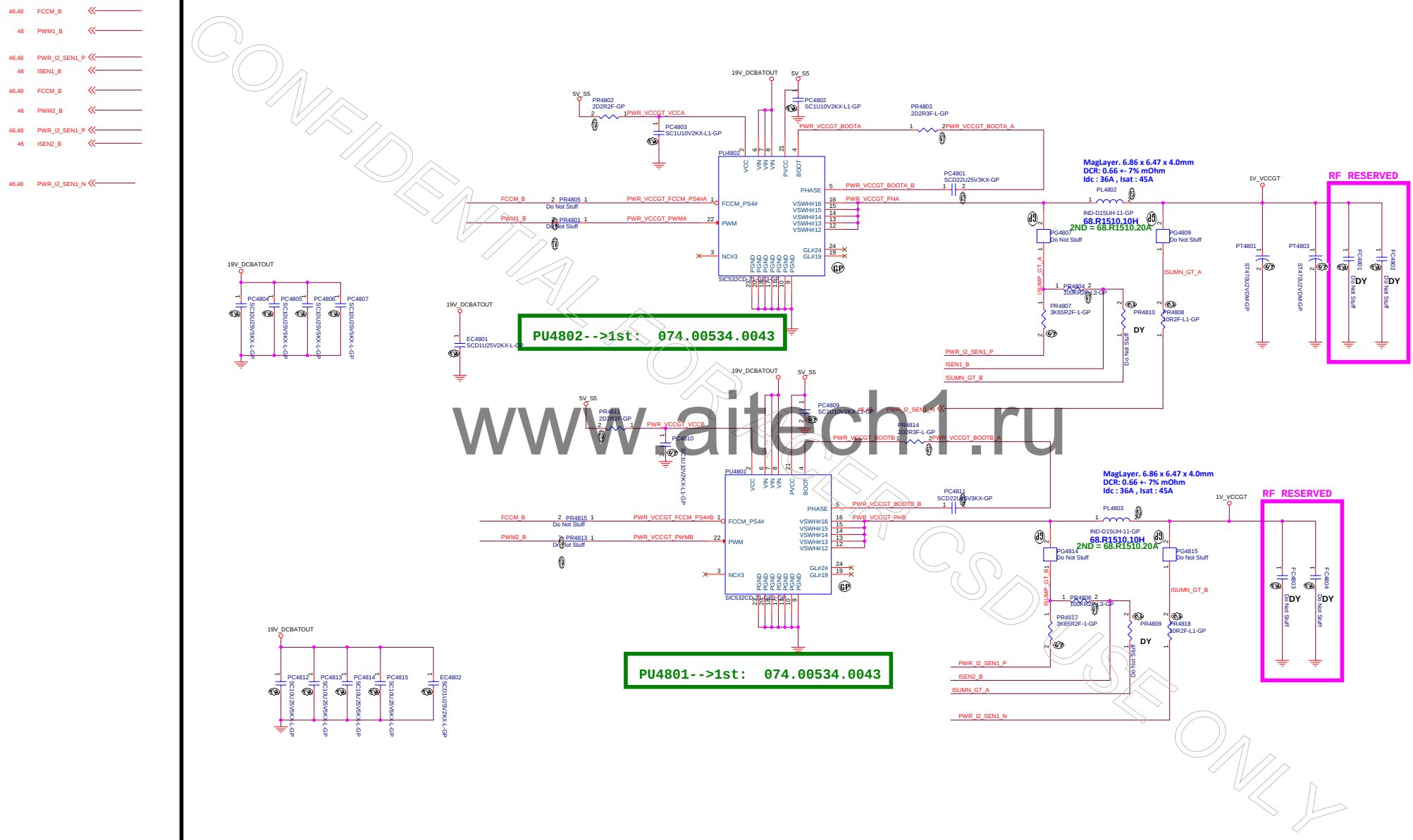
SKU1	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., HsiChih, Taipei Hsien 221, Taiwan, R.O.C.
File	RT6575D_5V/3D3V
Size: A1	Document Number: Uranus_KLS
Rev	-2
Date: Tuesday, January 17, 2017	Sheet 45 of 105


PROG1 - PR4612 : 110K -> VBOOT 0V / Slew Rate : 30mV/us / VRA:IA,VR2:GT,VR3:SA
PROG2 - PR4613 : 34K -> VRA IMAX:70A / VRA 2 Phase
PROG3 - PR4614 : 16K9 -> VRB IMAX:50A / VRB 2 Phase
PROG4 - PR4615 : 182K -> Droop Active / VRA & VRB FREQ 750KHz
PROG5 - PR4616 : 121K -> VRC IMAX 13A / VRC FREQ 750KHz
PU4601-->1st: 074.95829.0B73
www.aitech1.ru
CONFIDENTIAL
INTERNAL USE ONLY
Wistron Corporation
ISL95855_CPU_VCORE(1/3)
Uranus KLS
-2



SKU1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SIC631CD_CPU_VCORE(2/3)	
Size A2	Document Number: Uranus_KLS	Rev -2
Date: Tuesday, January 17, 2017	Sheet 47 of 105	



SKU1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SIC631CD_CPU_VCCGT(2/3)		
Size: A2	Document Number: Uranus_KLS	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 48 of 105	

SKU1

緯創資通

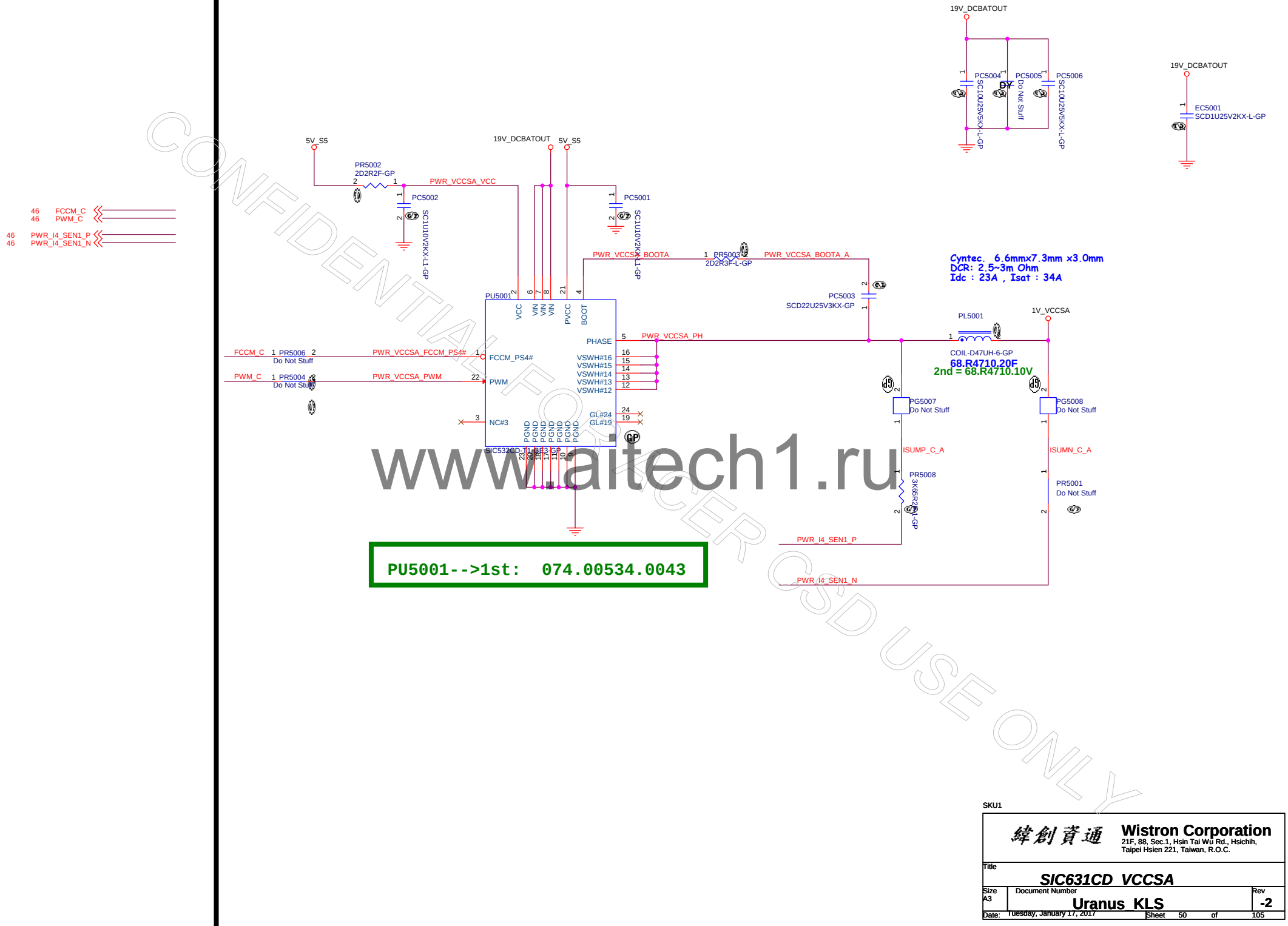
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

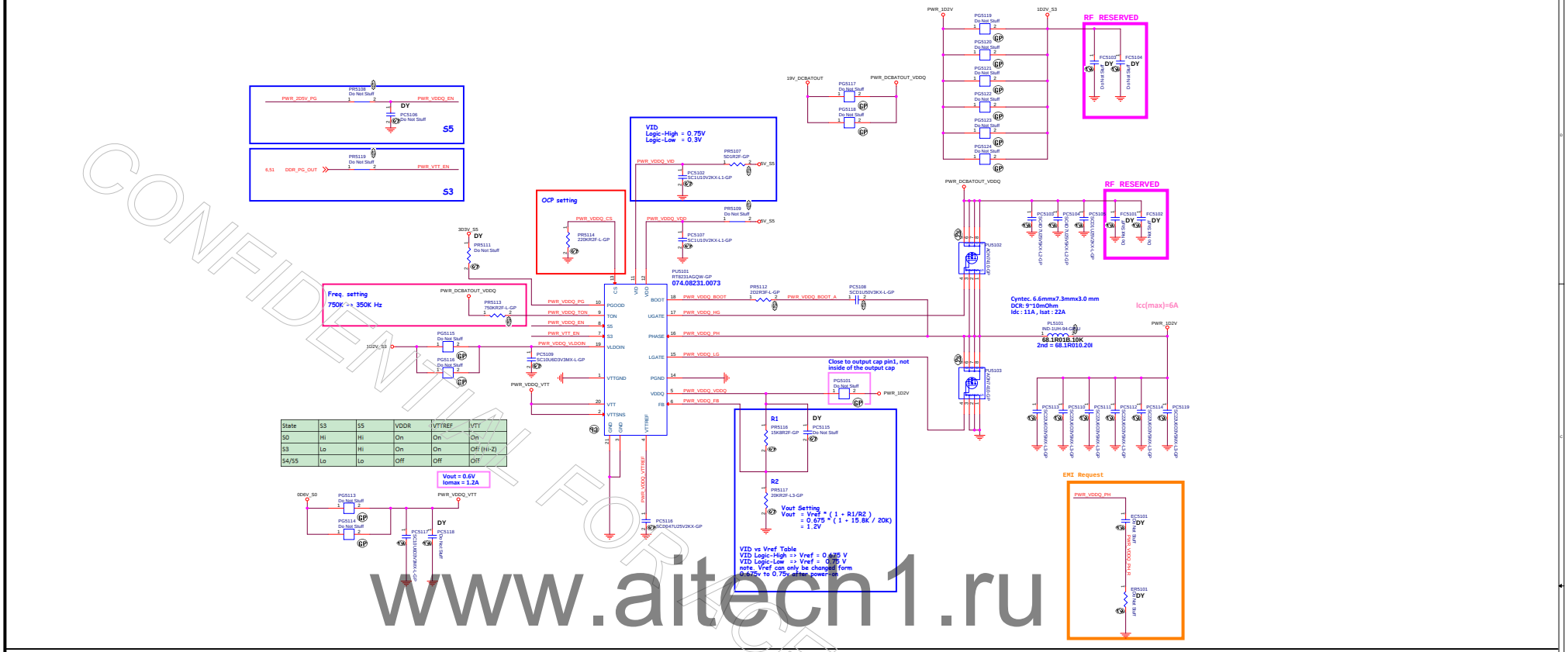
Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

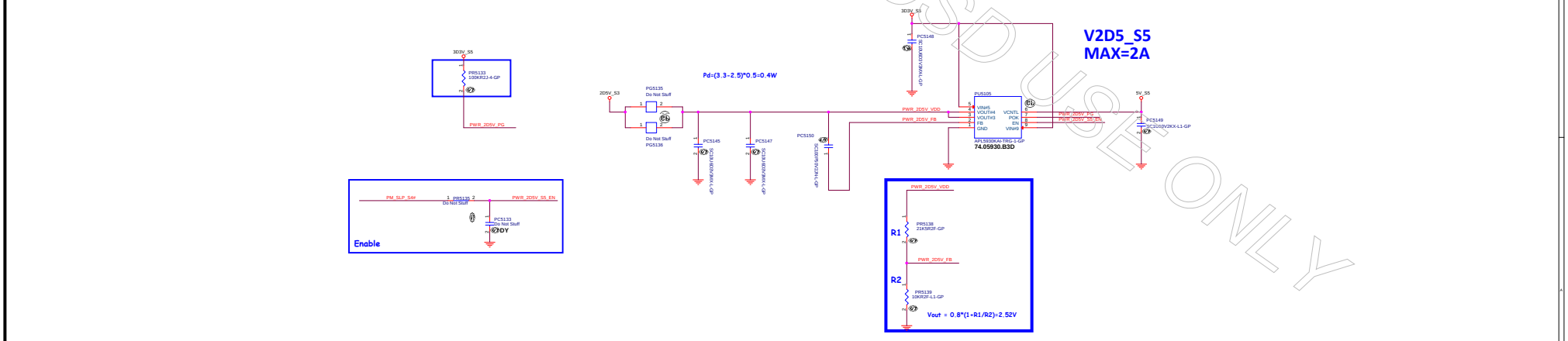
Date: Tuesday, January 17, 2017 Sheet 49 of 105



SKU1

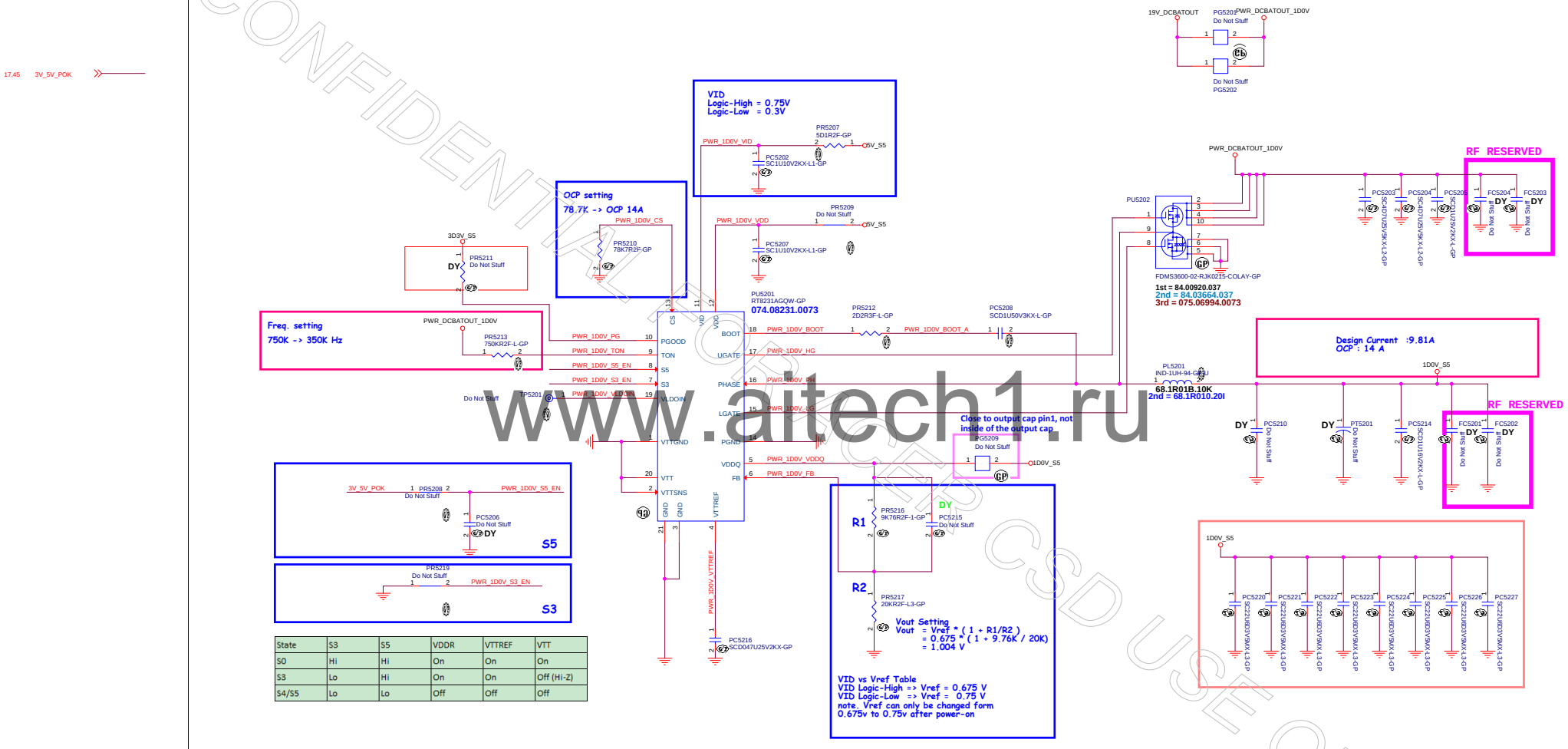
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *SIC631CD VCCSA*		
Size: A3	Document Number: Uranus KLS	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 50 of 105	





SKU1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., HsiChih, Taipei Hsien 221, Taiwan, R.O.C.		
File: RT8231_1D2V		
Size: A1	Document Number: Uranus_KLS	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 51 of 105	



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

SKU1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8231_1D0V

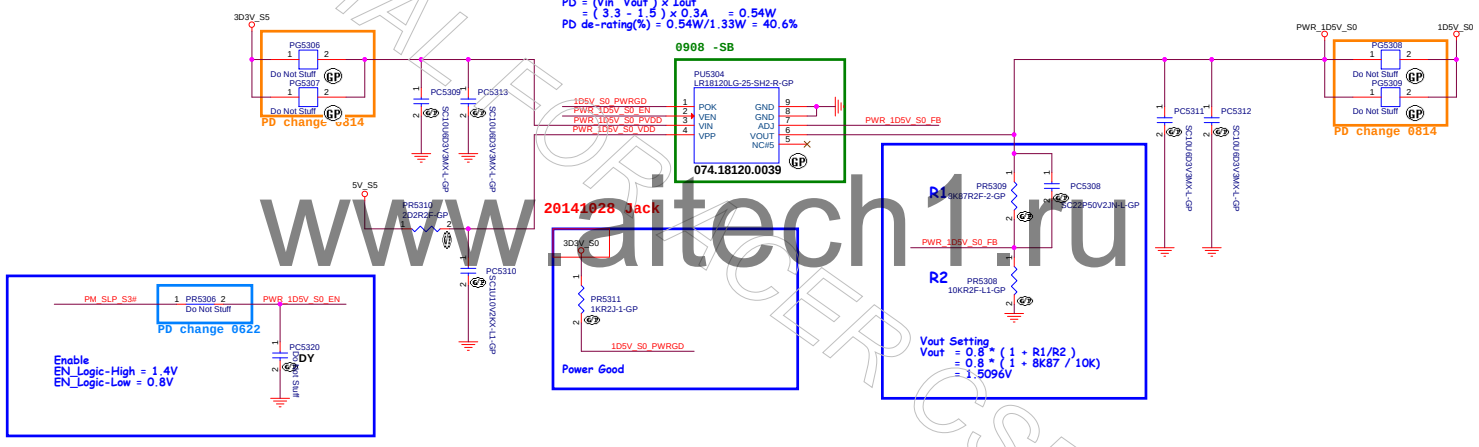
Size: A2 | Document Number: Uranus_KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 52 of 105

40 1D5V_S0_PWRGD

17,24,40,71 PM_SLP_S3#

1D5V_S0



SKU1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RT9025_1D5V	
Size A2	Document Number Uranus_KLS	Rev -2
Date: Tuesday, January 17, 2017	Sheet 53 of 105	

SKU1

緯創資通

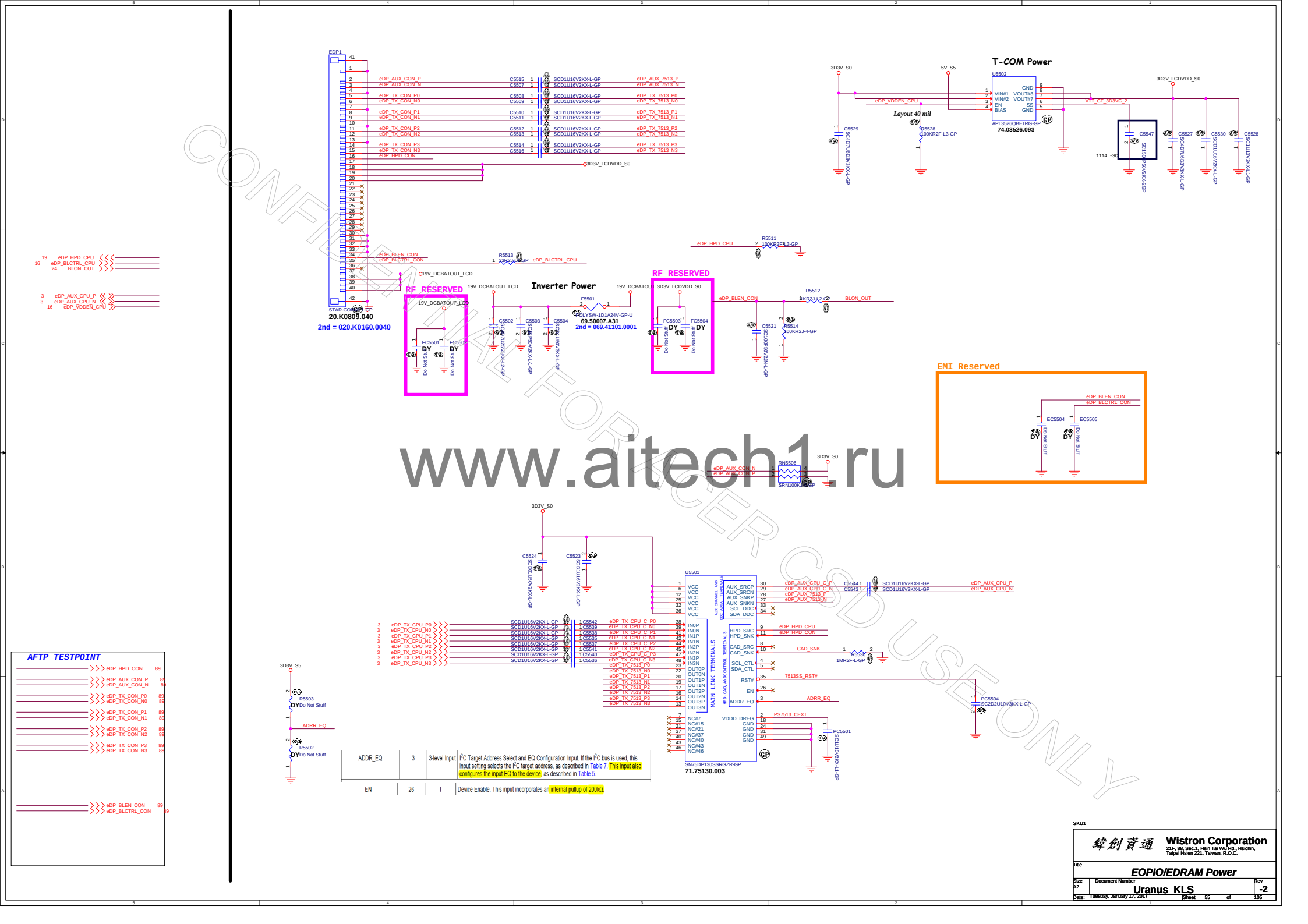
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 54 of 105


T-COM Power
Inverter Power
RF RESERVED
RF RESERVED
EMI Reserved
AFTP TESTPOINT
Layout 40 mil
20.K0809.040
2nd = 020.K0160.0040
69.50007.A31
2nd = 069.41101.0001
74.03526.093
71.75130.003
ADDR_EQ | 3 | 3-level Input | I²C Target Address Select and EQ Configuration Input. If the I²C bus is used, this input setting selects the I²C target address, as described in Table 7. This input also configures the input EQ to the device, as described in Table 5.
EN | 26 | I | Device Enable. This input incorporates an internal pullup of 200kΩ.
CONFIDENTIAL FOR WISTRON CD USE ONLY
www.aitech1.ru
SKU1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
EOPIO/EDRAM Power
Size A2
Document Number
Uranus_KLS
Rev -2
Date: Tuesday, January 17, 2017
Sheet 55 of 105

SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

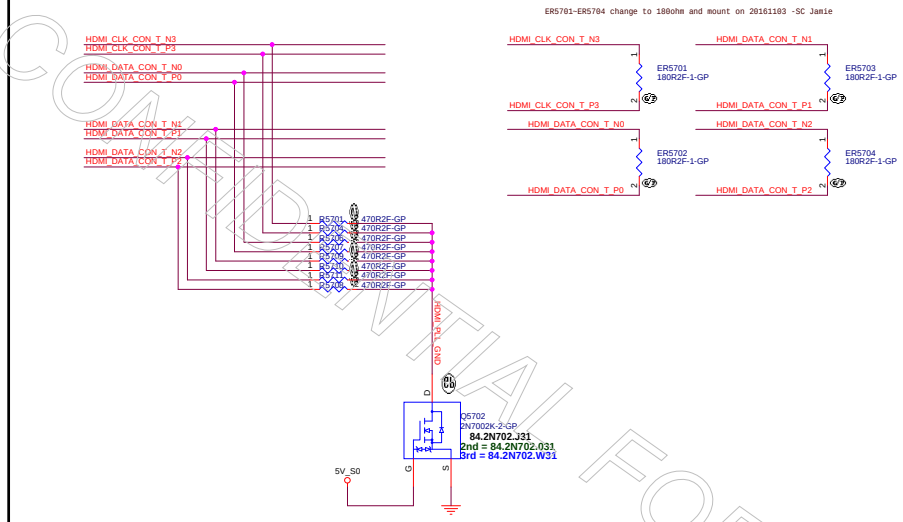
(Reserved)

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

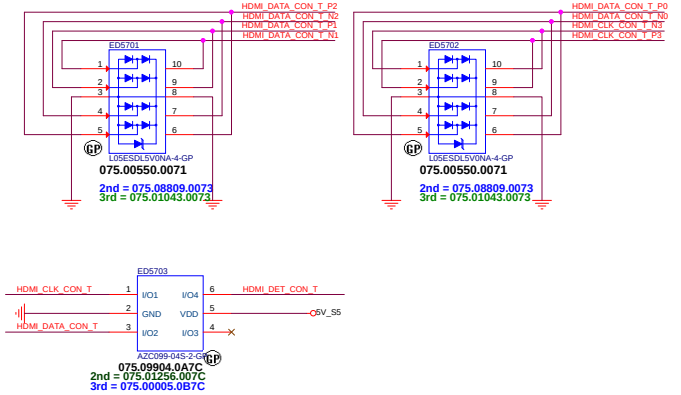
Date: Tuesday, January 17, 2017 Sheet 56 of 105

SSID = VIDEO

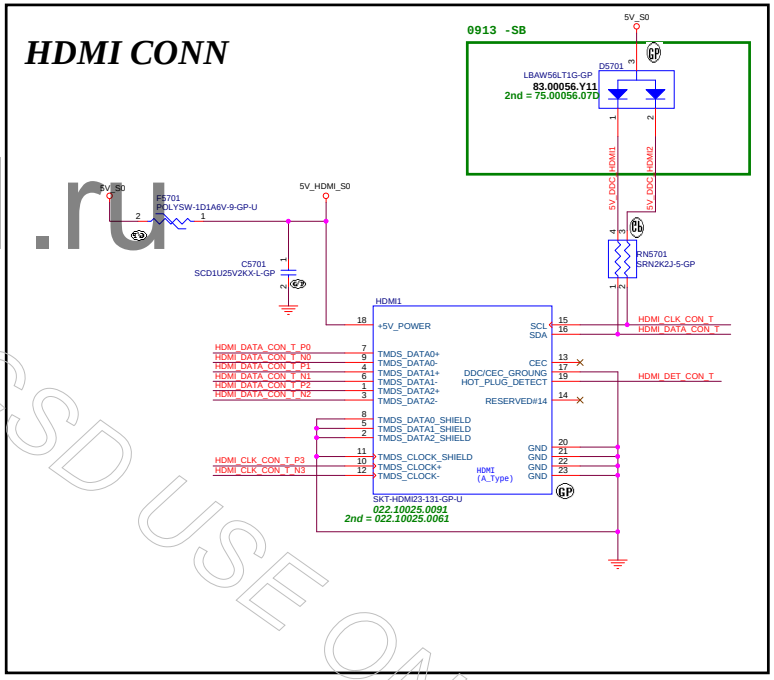
HDMI Level Shifter & CONNECTOR



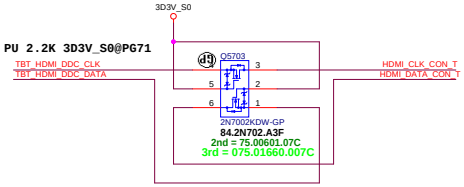
HDMI TVS -2 20170110



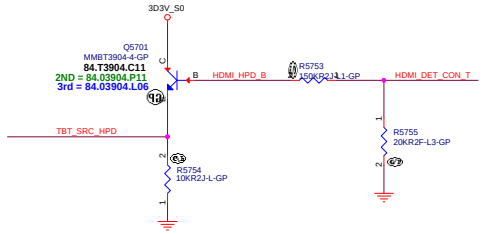
HDMI CONN



DDC BUS



HOT PLUG



455.0BP01.0001

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDMI Level Shifter/Conn		
Size: A2	Document Number: Uranus_KLS	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 57 of 105	

SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 58 of 105

SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 59 of 105

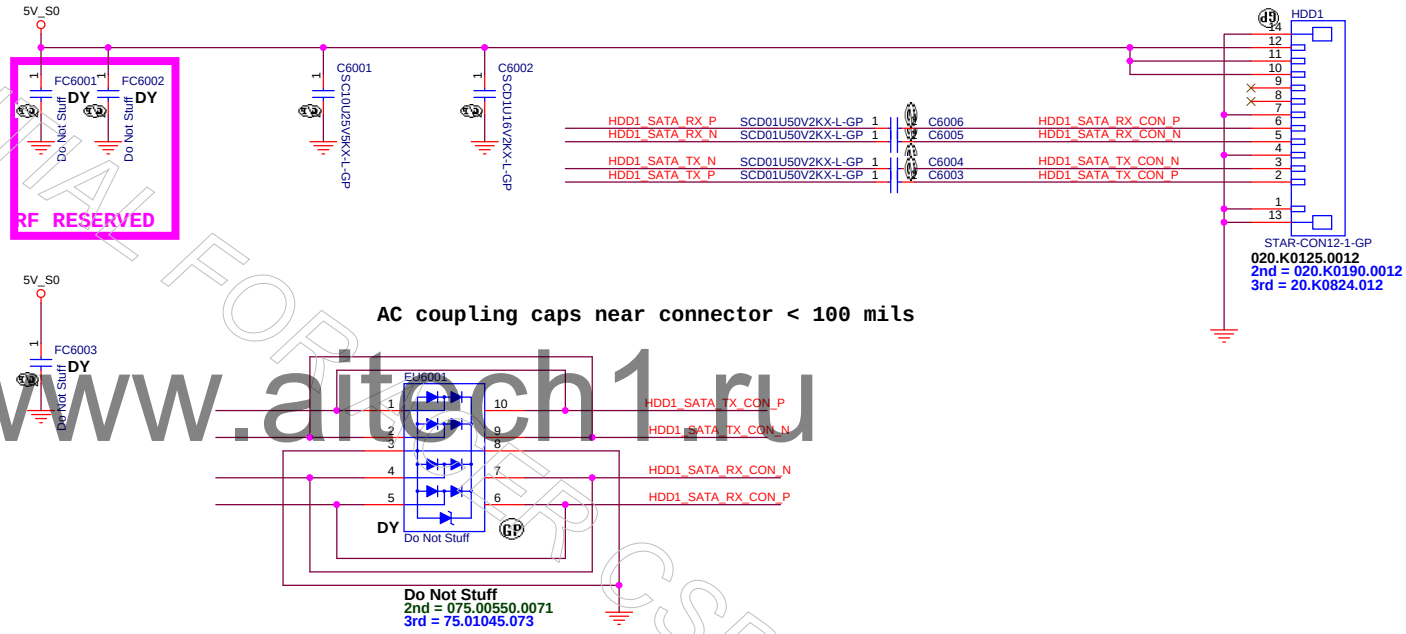
16 HDD1_SATA_RX_N
16 HDD1_SATA_RX_P
16 HDD1_SATA_TX_N
16 HDD1_SATA_TX_P

SSID = SATA

SATA HDD1 Connector

AFTP TESTPOINT

89 HDD1_SATA_TX_CON_P
89 HDD1_SATA_TX_CON_N
89 HDD1_SATA_RX_CON_P
89 HDD1_SATA_RX_CON_N



SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

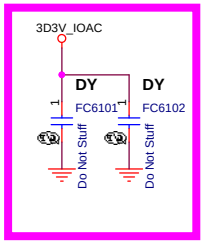
Size: A3 | Document Number: Uranus_KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 60 of 105

SSID = Wireless/ Wigig

NGFF Connector (802.11a/b/g/n)

RF RESERVED



19 WIFI_RF_EN
19,61,89 BLUETOOTH_EN
14,24,31,63,68,71,79,89,91 PLT_RST#

24,68 E51_TXD

15 BT_USB20_N
15 BT_USB20_P

17,31,63,71 PCIE_WAKE#
18,61,89 WLAN_CLKREQ_CPU#

18,61,89 WLAN_CLK_CPU#
18,61,89 WLAN_CLK_CPU

15,61,89 WLAN_PCIE_RX_N
15,61,89 WLAN_PCIE_RX_P

15 WLAN_PCIE_TX_N
15 WLAN_PCIE_TX_P

AFTP TESTPOINT

PCIE_WAKE#_WLAN 89
WLAN_CLKREQ_CPU# 18,61,89

WLAN_CLK_CPU# 18,61,89
WLAN_CLK_CPU 18,61,89

WLAN_PCIE_RX_N 15,61,89
WLAN_PCIE_RX_P 15,61,89

WLAN_PCIE_TX_CON_N 89
WLAN_PCIE_TX_CON_P 89

BT_USB20_N_R 89
BT_USB20_P_R 89

WIFI_RF_EN_CON 89
BLUETOOTH_EN 19,61,89
WLAN_RST# 89

E51_TXD_R 89

SKU1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Mini card-WLAN***		
Size: A3	Document Number: **Uranus_KLS**	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 61 of 105	

SSID = Wireless

SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

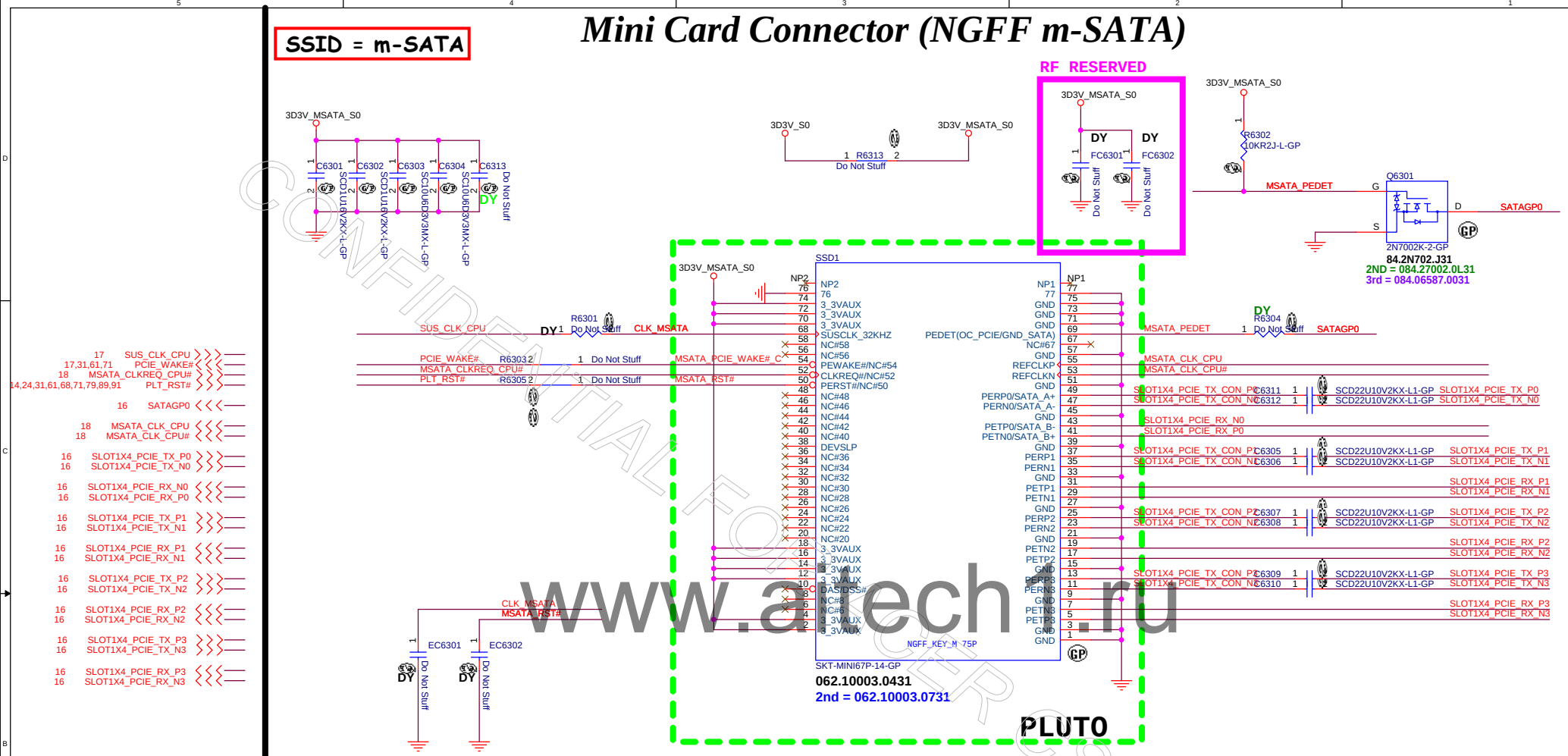
Title: ***(Reserved)WWAN***

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 62 of 105

Mini Card Connector (NGFF m-SATA)

SSID = m-SATA



17 SUS_CLK_CPU
17,31,61,71 PCIE_WAKE#
18 MSATA_CLKREQ_CPU#
14,24,31,61,68,71,79,89,91 PLT_RST#
16 SATAGP0
18 MSATA_CLK_CPU
18 MSATA_CLK_CPU#
16 SLOT1X4_PCIE_TX_P0
16 SLOT1X4_PCIE_TX_N0
16 SLOT1X4_PCIE_RX_N0
16 SLOT1X4_PCIE_RX_P0
16 SLOT1X4_PCIE_TX_P1
16 SLOT1X4_PCIE_TX_N1
16 SLOT1X4_PCIE_RX_P1
16 SLOT1X4_PCIE_RX_N1
16 SLOT1X4_PCIE_TX_P2
16 SLOT1X4_PCIE_TX_N2
16 SLOT1X4_PCIE_RX_P2
16 SLOT1X4_PCIE_RX_N2
16 SLOT1X4_PCIE_TX_P3
16 SLOT1X4_PCIE_TX_N3
16 SLOT1X4_PCIE_RX_P3
16 SLOT1X4_PCIE_RX_N3

Table 34-5. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

SKU1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SSD-NGFF		
Size: A3	Document Number: Uranus_KLS	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 63 of 105	

SSID = User.Interface

24 LB_PWM
24,65,89 KBC_PWRBTN#

5V_S5

LB1
ACES-CON4-29-GP
20.F1639.004
2nd = 020.F0700.0004
3rd = 20.F1804.004

LB_PWM_LED1
LB_PWM_LED2
R6401 1 2 200R2F-L1-GP
R6402 1 2 200R2F-L1-GP
LB_PWM_R

Q6403
2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.06587.0031

LB_PWM
C6401
SCD1U16V2KX-L-GP

EMI Reserved
LB_PWM_R
EC6401
DO NOT STUFF
Do Not Stuff
ENG 0422

Power Button

KBC_PWRBTN#
PW1
Do Not Stuff
Do Not Stuff
LAB
2nd = 62.40089.441
3rd = 62.40009.D71

AFTP TESTPOINT

89 LB_PWM_LED1
89 LB_PWM_LED2

SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

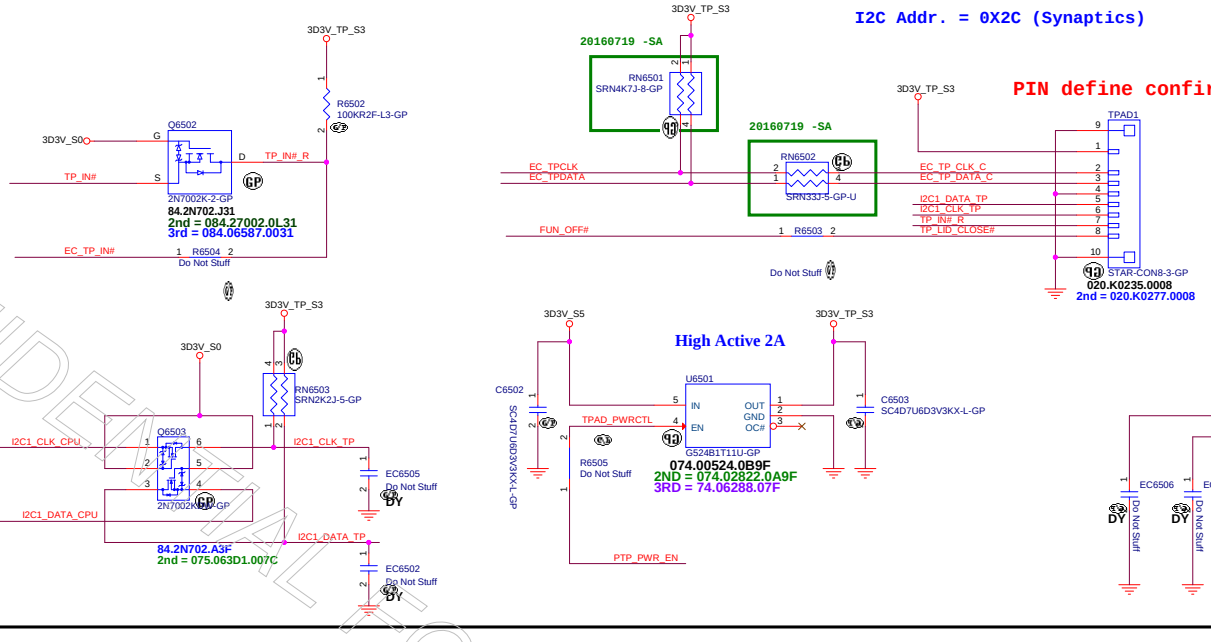
Title: LED Bard/Power Button

Size	Document Number	Rev
A4	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 64 of 105

Precision Touch Pad

I2C Addr. = 0X2C (Synaptics)



24,65 PTP_PWR_EN
19 KB_BL_DET
14 TP_IN#
24 EC_TP_IN#
19 I2C1_CLK_CPU
19 I2C1_DATA_CPU
24 EC_TPCLK
24 EC_TPDATA
24 FUN_OFF#
24,65 PTP_PWR_EN
24,64,89 KBC_PWRBTN#
24 KB_BL_EN

24,89 KROW[0..17]
24,89 KCOL[0..7]

24 CAPS_LED
24 NUMLOCK_LED

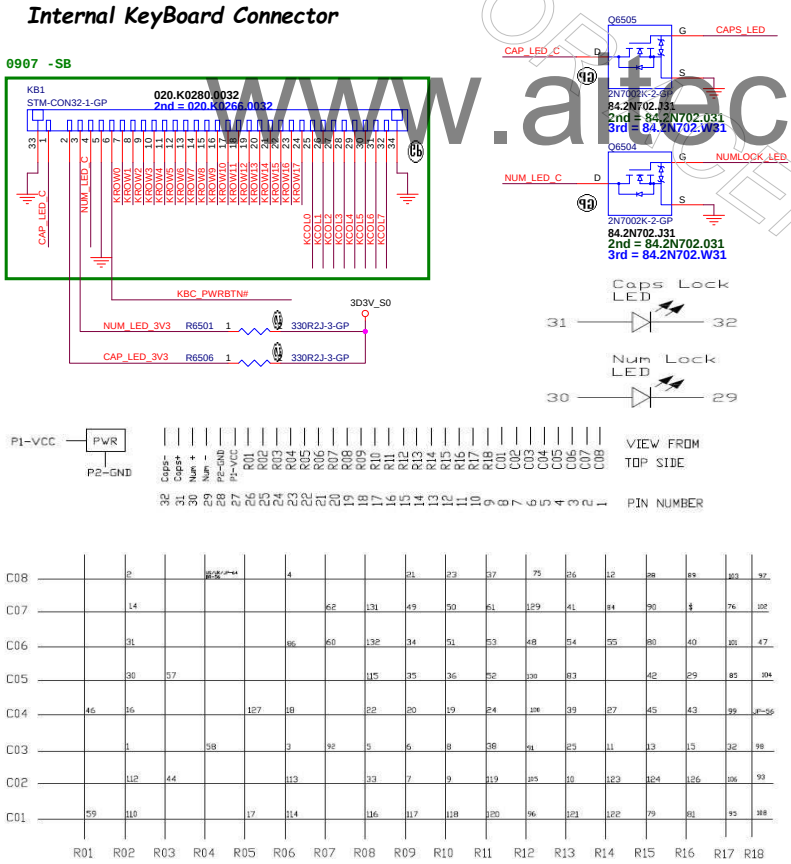
AFTP TESTPOINT

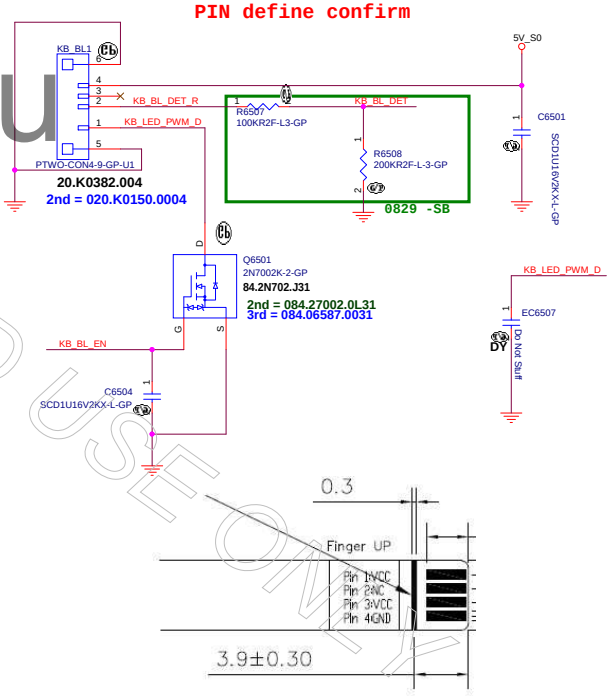
EC_TP_CLK_C 89
EC_TP_DATA_C 89
I2C1_DATA_TP 89
I2C1_CLK_TP 89
TP_IN#_R 89
TP_LID_CLOSE# 89

KB_BL_DET_R 89
KB_LED_PWM_D 89
NUM_LED_3V3 89
CAP_LED_3V3 89
NUM_LED_C 89
CAP_LED_C 89

AFTP TEST POINT

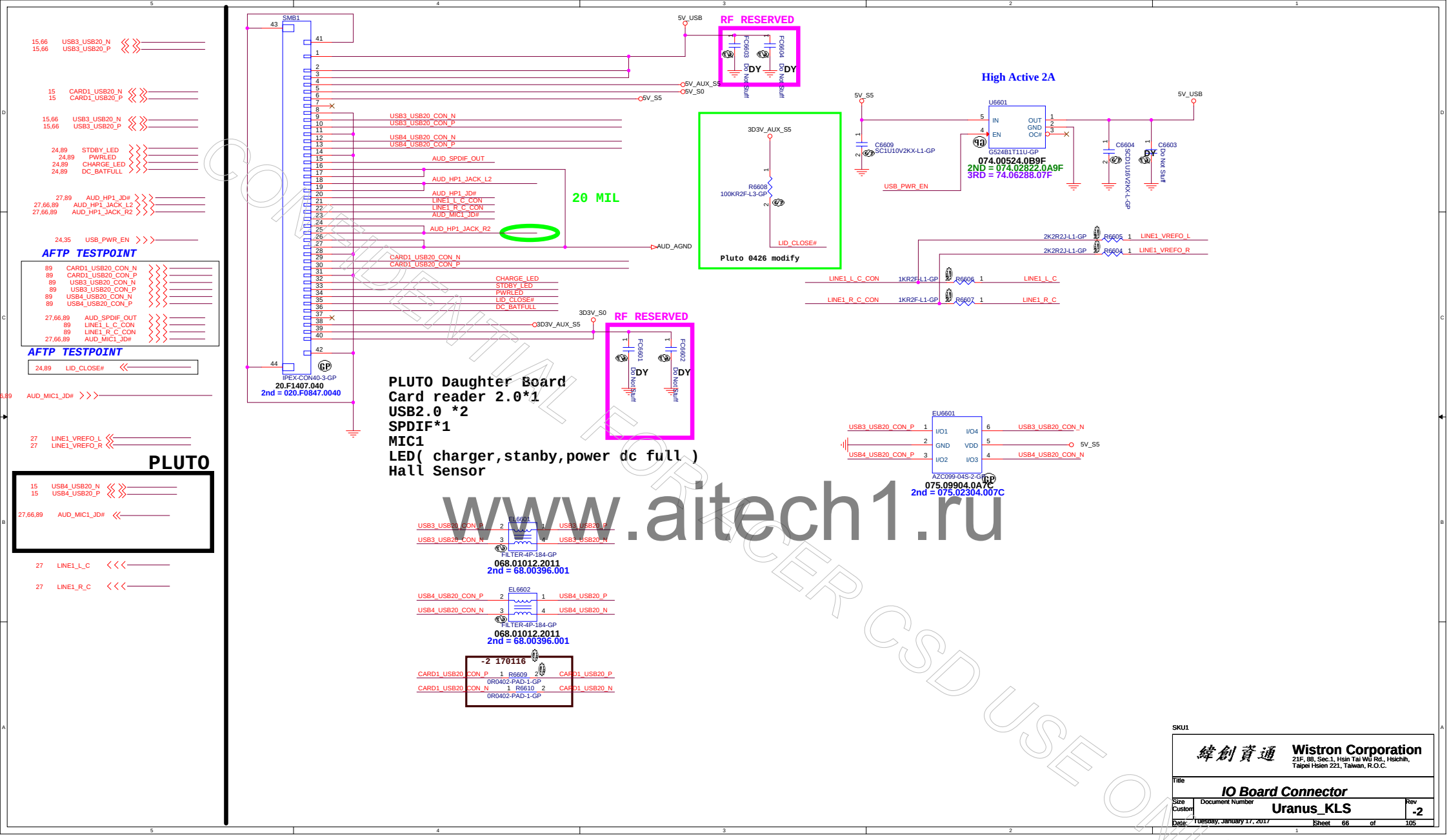
Internal KeyBoard Connector





SKU1

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LED Bard / Power Button
Size: Custom	Document Number: Uranus_KLS
Rev	-2
Date: Tuesday, January 17, 2017	Sheet 65 of 105



SKU1

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	IO Board Connector
Size: Custom	Document Number: Uranus_KLS
Rev: -2	
Date: Tuesday, January 17, 2017	Sheet 66 of 105

SKU1

緯創資通

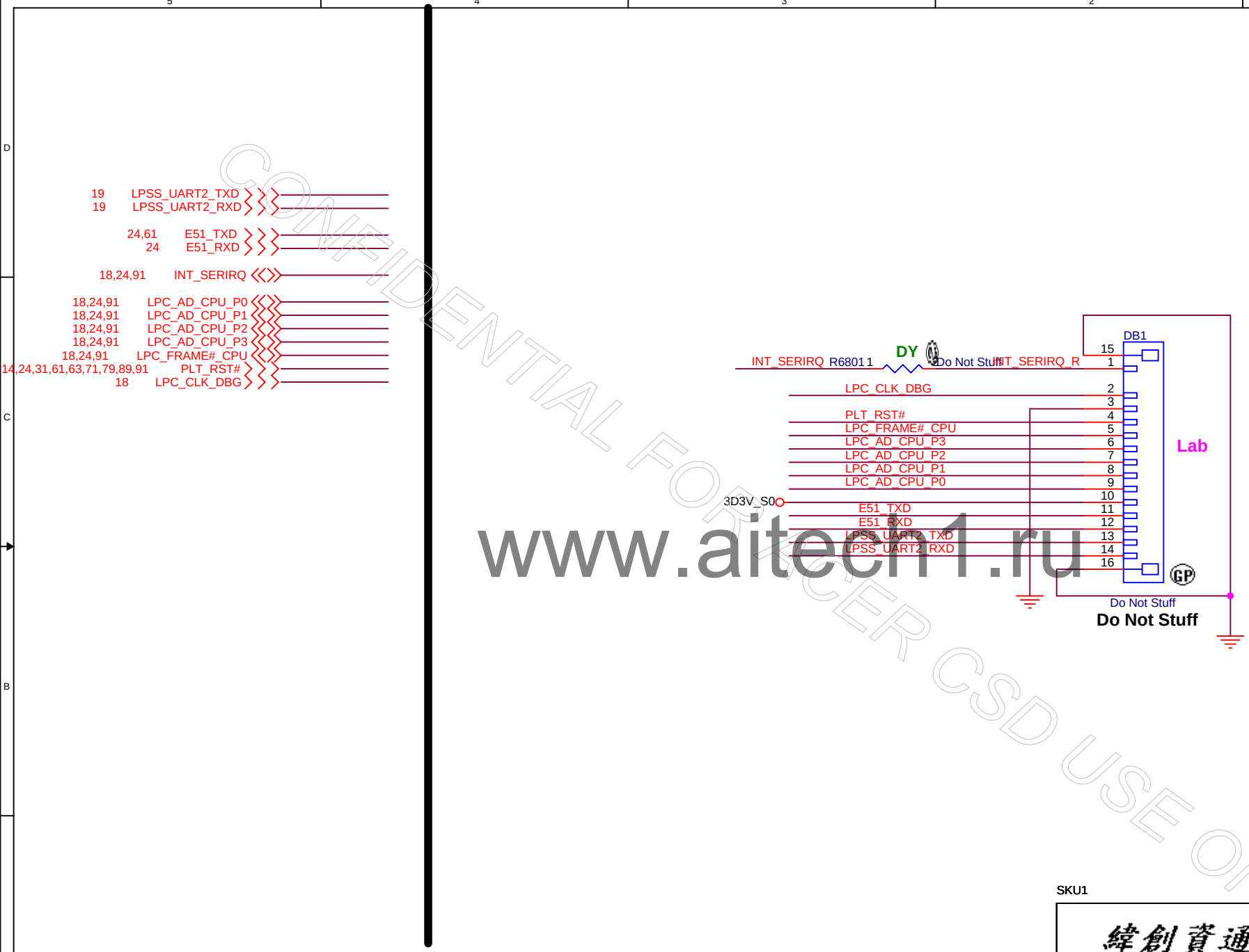
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 67 of 105



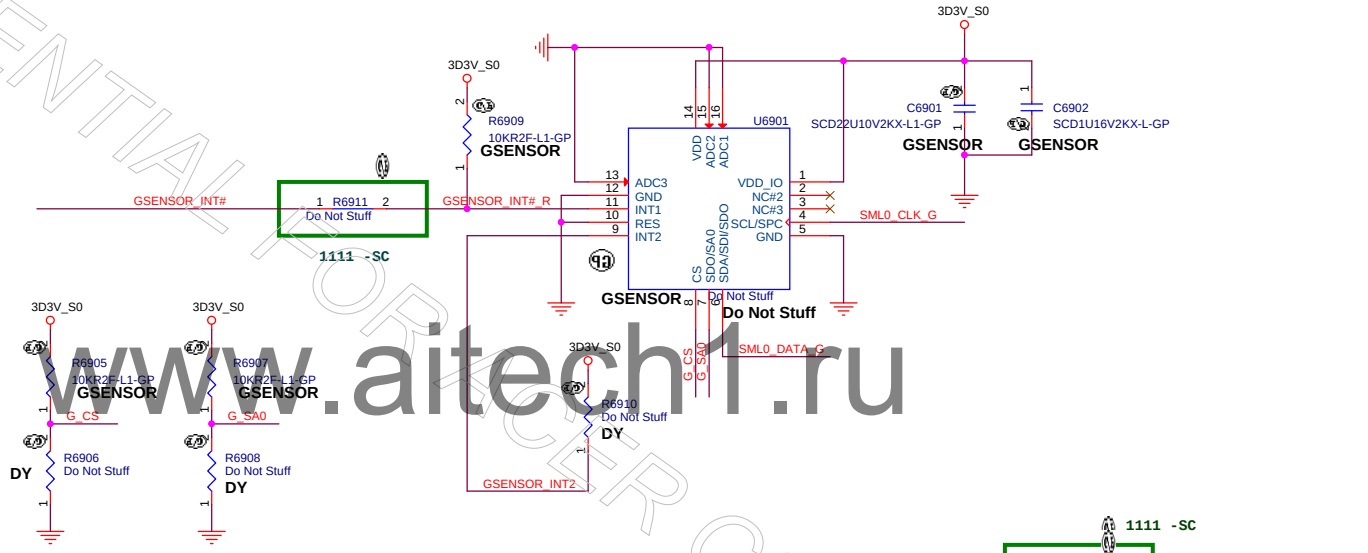
SKU1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **Debug connector**		
Size: A4	Document Number: **Uranus_KLS**	Rev: **-2**
Date: Tuesday, January 17, 2017	Sheet 68 of 105	

SSID = User.Interface

G Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

SKU1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	G-SENSOR
Size A3	Document Number: Uranus_KLS
Rev	-2
Date: Tuesday, January 17, 2017	Sheet 69 of 105

SKU1

緯創資通

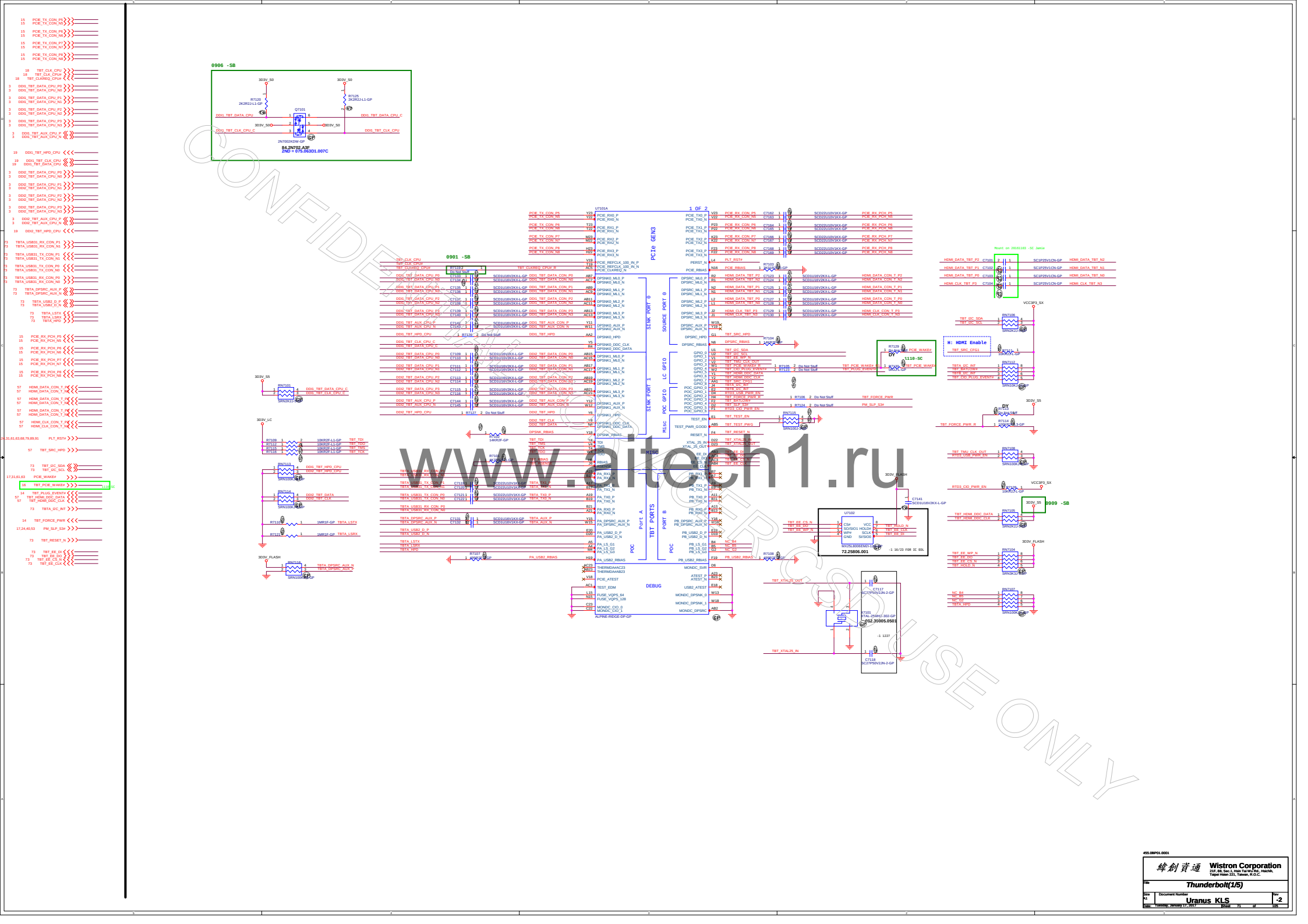
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

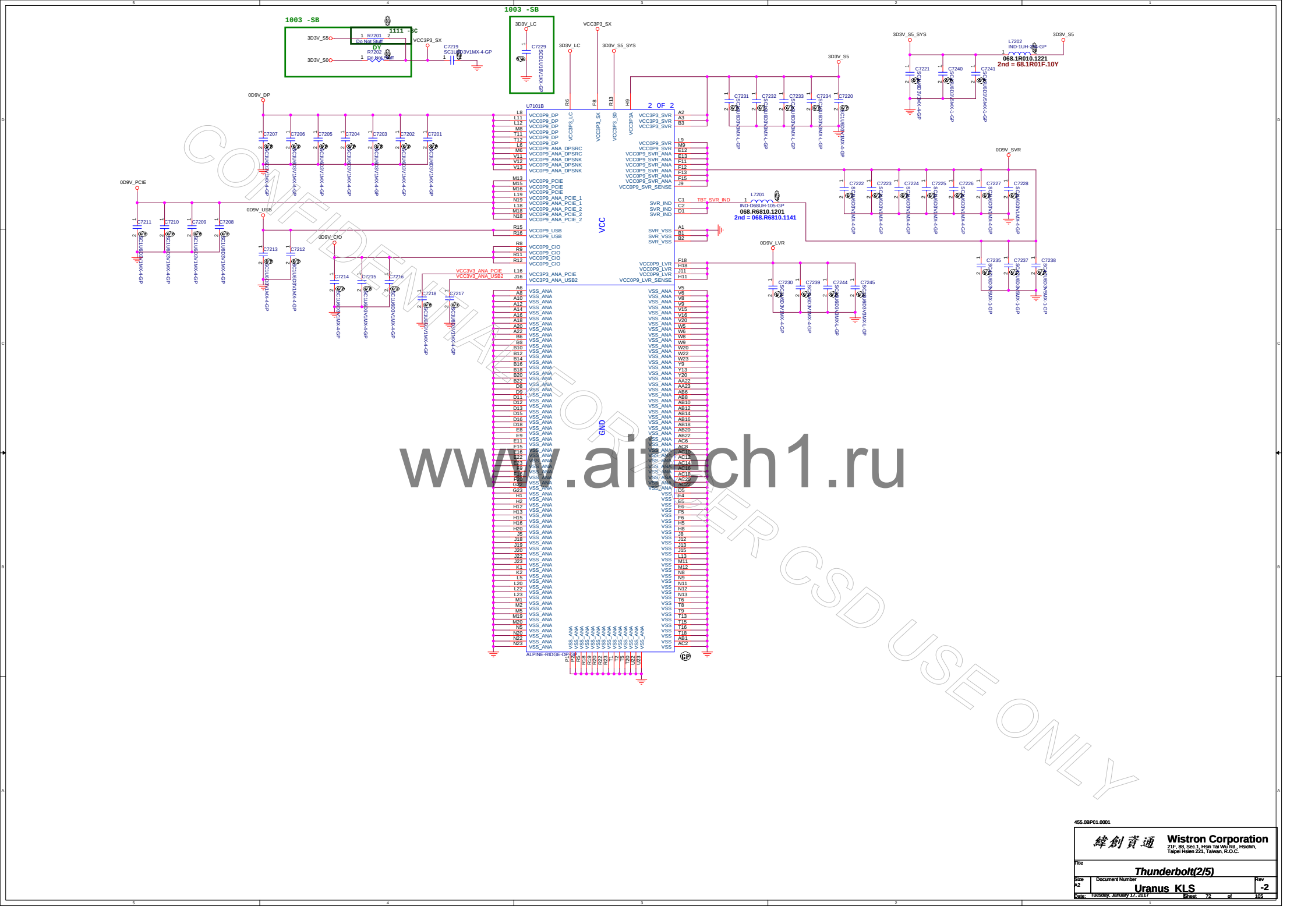
Title

(Reserved)Free Fall Sensor

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 70 of 105


0906 -SB
0901 -SB
0909 -SB
U7101A
1 OF 2
PCIe GEN3
SINK PORT 0
SOURCE PORT 0
SINK PORT 1
LC GPIO
POC GPIO
Misc
MISC
TBT PORTS
Port A
Port B
POC
DEBUG
ALPINE-RIDGE-DP-GP
Thunderbolt(1/5)
Uranus KLS
-2
Wistron Corporation
455.0BP01.0001
CONFIDENTIAL
www.aitech1.ru



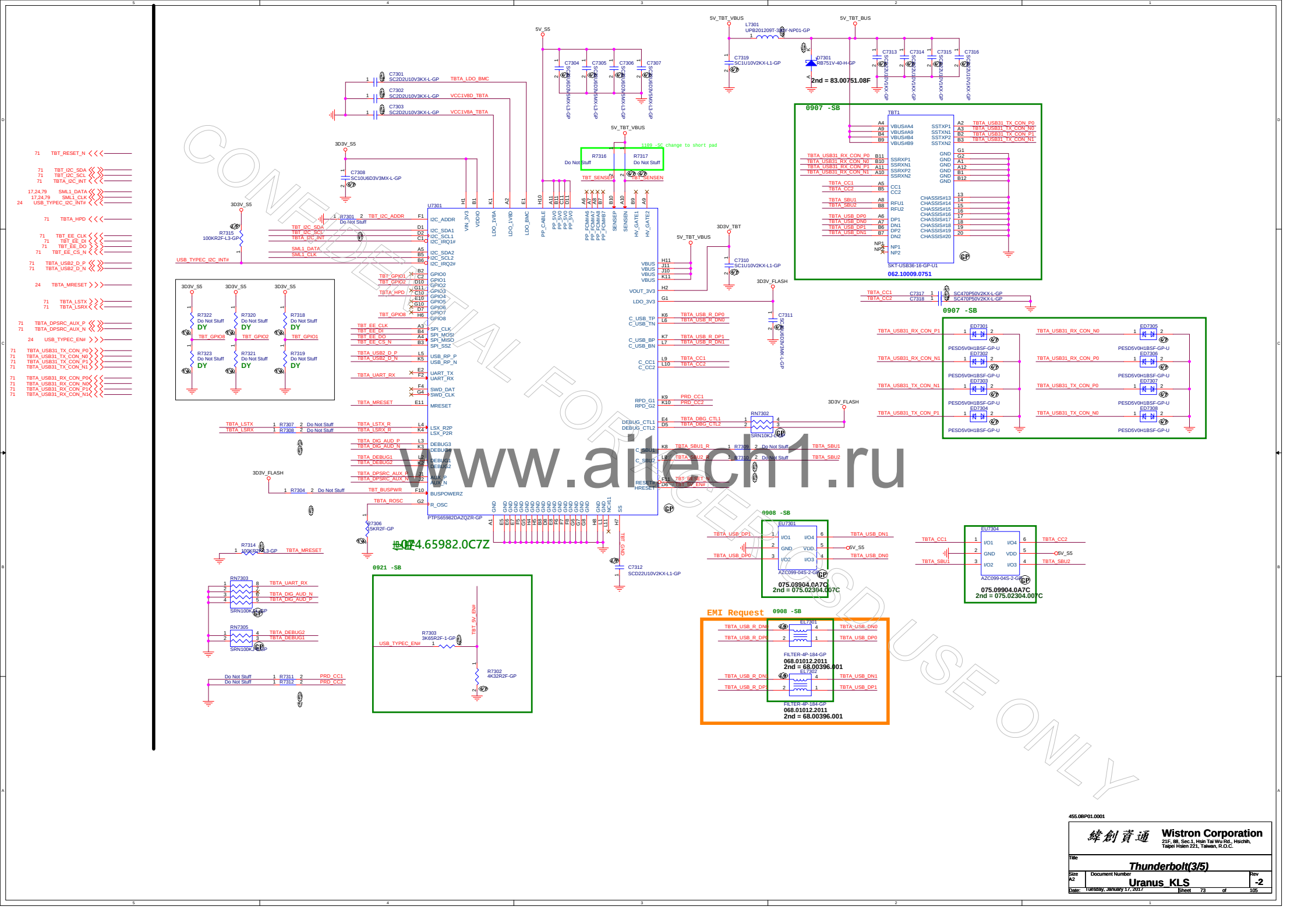
455.0BP01.0001

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thunderbolt(2/5)

Size: A2 | Document Number: Uranus KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 72 of 105



455.0BP01.0001

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Thunderbolt(3/5)
Size A2	Document Number Uranus_KLS
Rev	-2
Date: Tuesday, January 17, 2017	Sheet 73 of 105

SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)Thunderbolt (4/5)***

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 74 of 105

SKU1

緯創資通

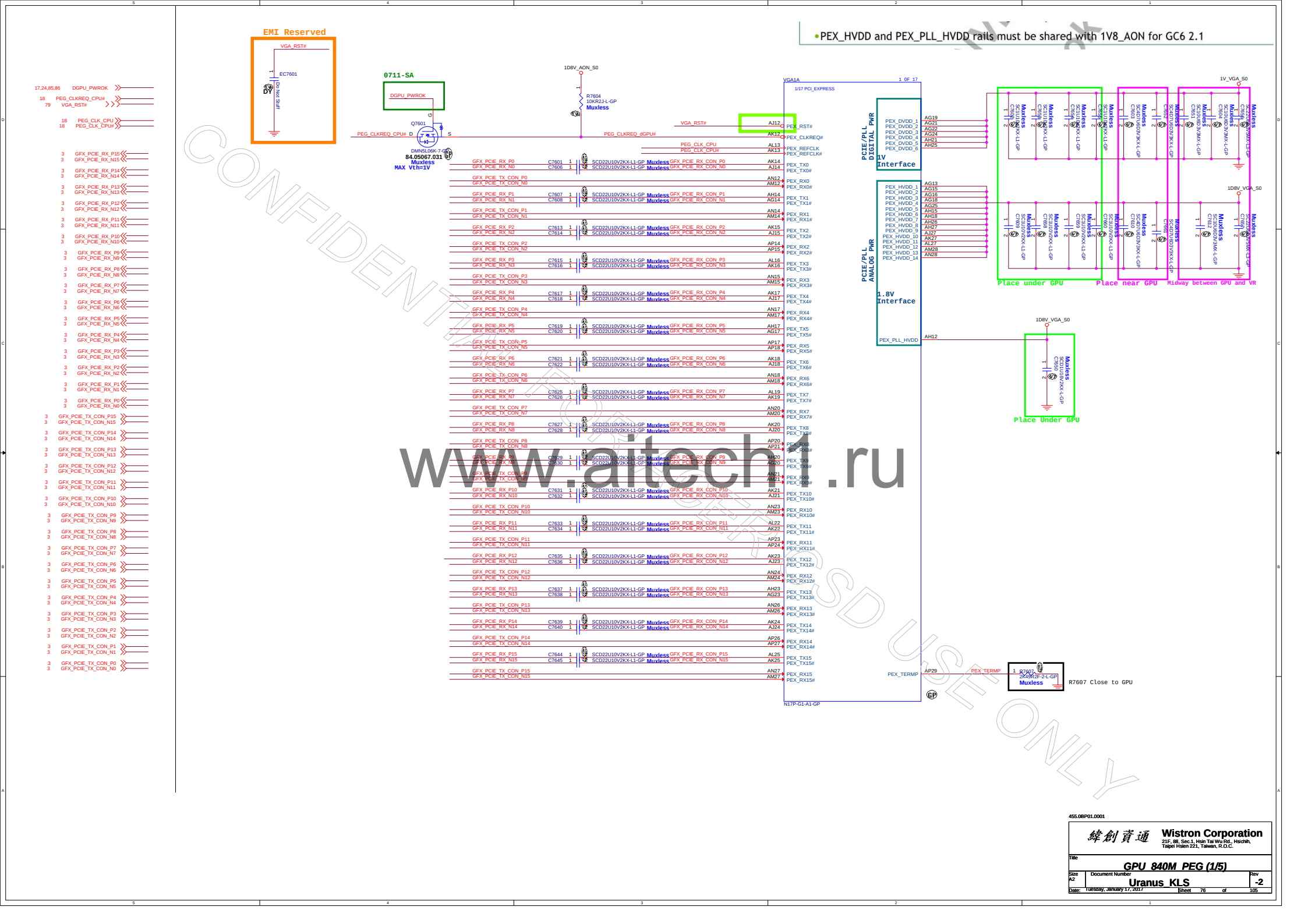
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)Thunderbolt (5/5)

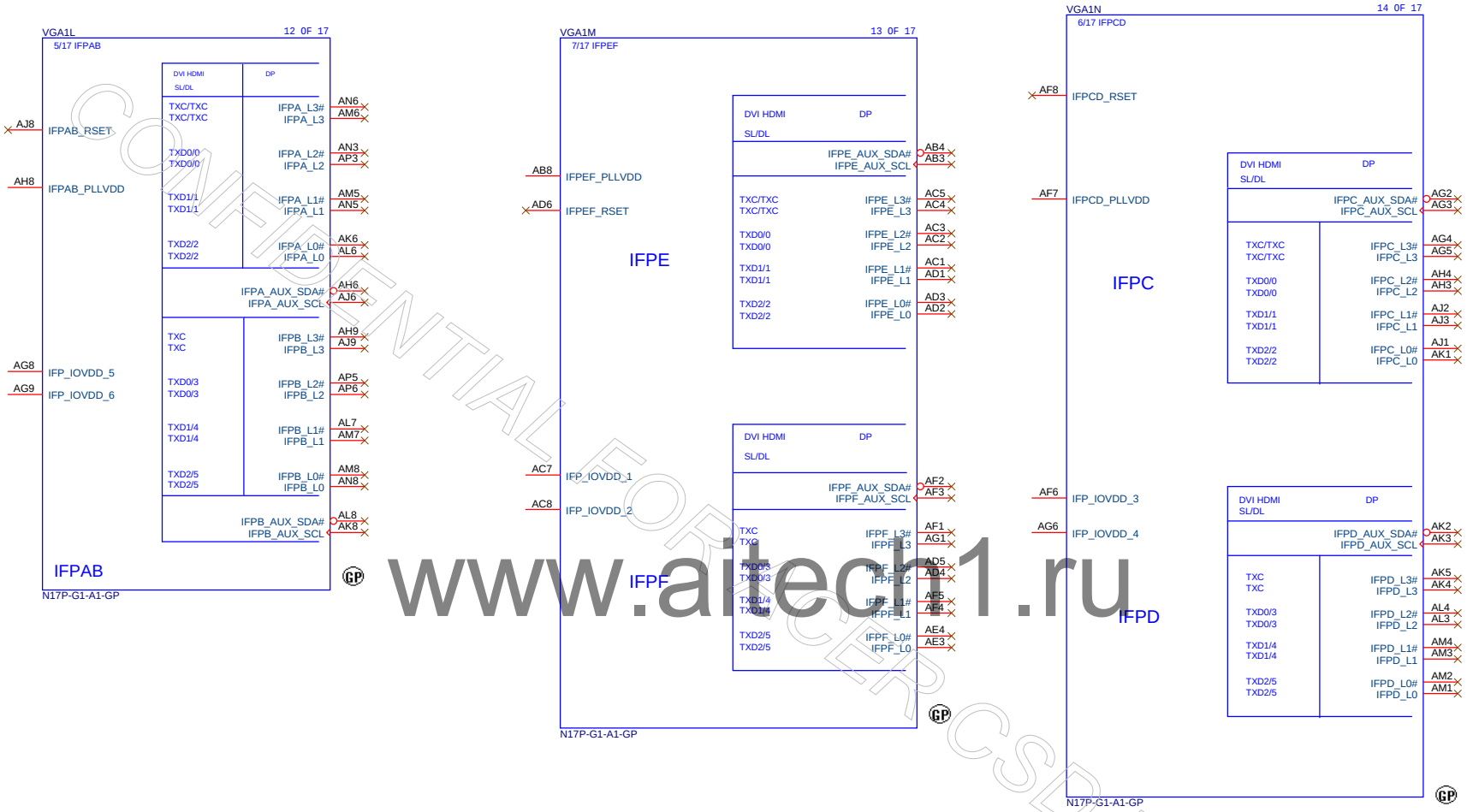
Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 75 of 105



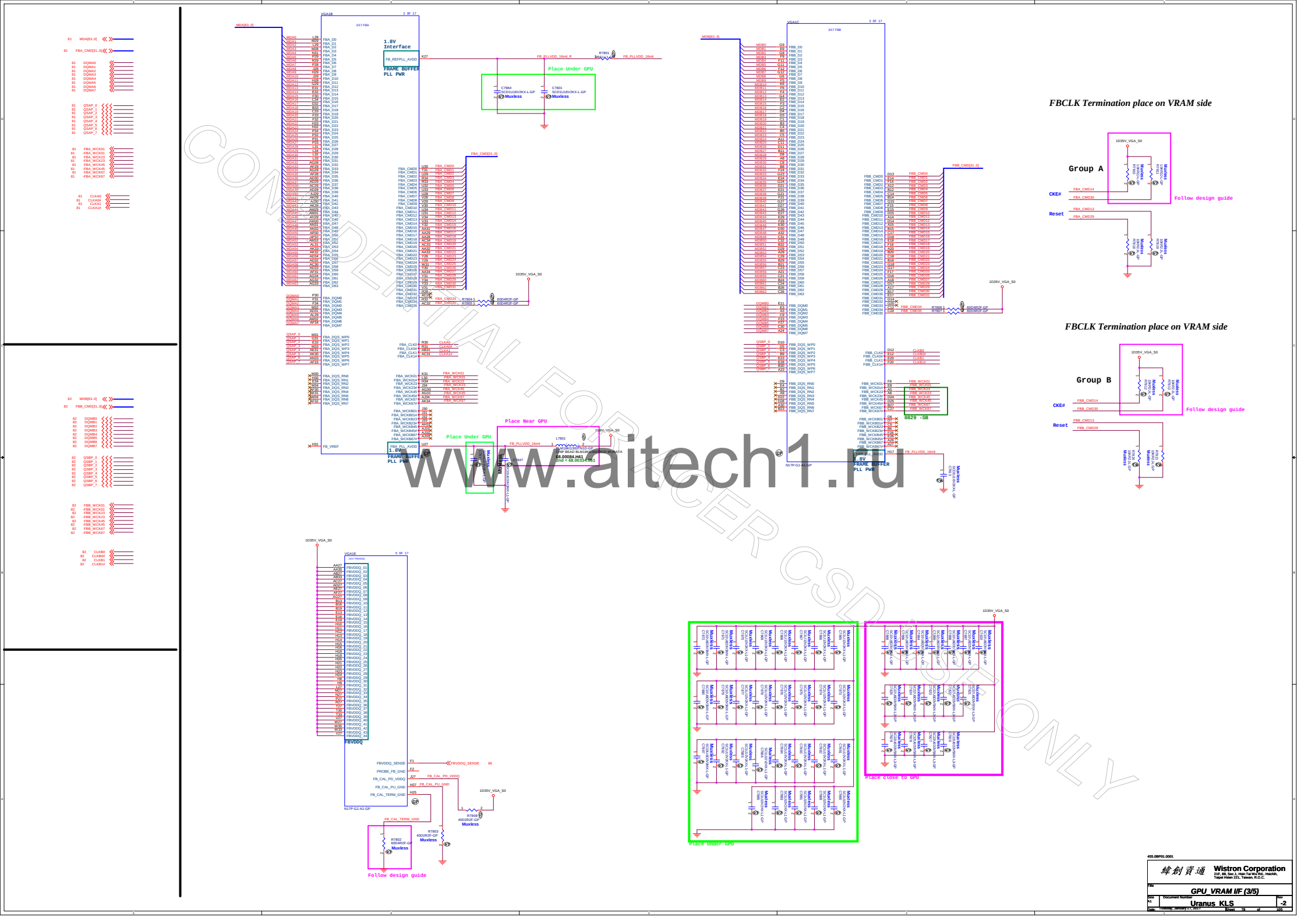
455.0BP01.0001

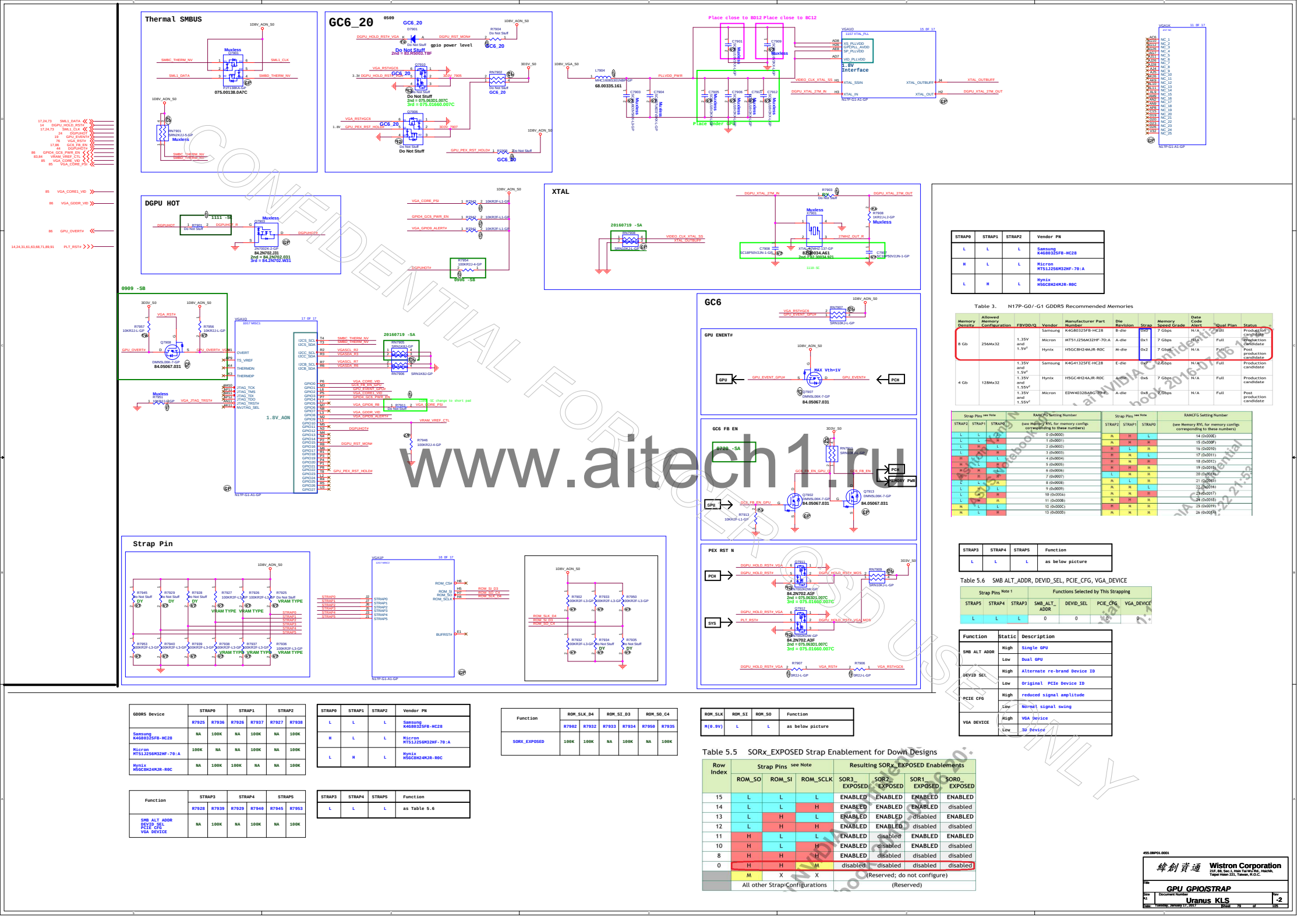
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GPU_840M_PEG (1/5)
Size A2	Document Number Uranus_KLS
Rev	-2
Date: Tuesday, January 17, 2017	Sheet 76 of 105



455.0BP01.0001

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU_DIGITALOUT (2/5)		
Size: A3	Document Number: Uranus_KLS	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 77 of 105	





STRAP0	STRAP1	STRAP2	Vendor PN
L	L	L	Samsung K4G80325FB-HC28
H	L	L	Micron MT51J256M32HF-70:A
L	H	L	Hynix H5GC8H24MJR-R0C

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V[2]	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production candidate
4 Gb	128Mx32	1.35V and 1.5V[2]	Samsung	K4G41325FE-HC28	E-die	0x7	2.6bps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production candidate

Strap Pins see Note			RAMCFG Setting Number	Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)	M	H	L	14 (0x000E)
L	L	H	1 (0x0001)	M	H	H	15 (0x000F)
L	H	L	2 (0x0002)	H	L	M	16 (0x0010)
L	H	M	3 (0x0003)	H	M	L	17 (0x0011)
H	L	L	4 (0x0004)	H	M	H	18 (0x0012)
H	L	H	5 (0x0005)	H	H	M	19 (0x0013)
H	M	L	6 (0x0006)	L	M	M	20 (0x0014)
H	H	M	7 (0x0007)	L	H	M	21 (0x0015)
L	L	M	8 (0x0008)	M	L	M	22 (0x0016)
L	M	L	9 (0x0009)	M	M	L	23 (0x0017)
L	M	H	10 (0x000A)	M	H	H	24 (0x0018)
L	H	M	11 (0x000B)	M	H	M	25 (0x0019)
M	L	L	12 (0x000C)	H	M	M	26 (0x001A)
M	L	H	13 (0x000D)	M	M	M	

STRAP3	STRAP4	STRAP5	Function
L	L	L	as below picture

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Function	Static	Description
SMB ALT ADDR	High	Single GPU
	Low	Dual GPU
DEVID SEL	High	Alternate re-brand Device ID
	Low	Original PCIe Device ID
PCIE CFG	High	reduced signal amplitude
	Low	Normal signal swing
VGA DEVICE	High	VGA Device
	Low	3D Device

GDDR5 Device	STRAP0		STRAP1		STRAP2	
	R7925	R7936	R7926	R7937	R7927	R7938
Samsung K4G80325FB-HC28	NA	100K	NA	100K	NA	100K
Micron MT51J256M32HF-70:A	100K	NA	NA	100K	NA	100K
Hynix H5GC8H24MJR-R0C	NA	100K	100K	NA	NA	100K

STRAP0	STRAP1	STRAP2	Vendor PN
L	L	L	Samsung K4G80325FB-HC28
H	L	L	Micron MT51J256M32HF-70:A
L	H	L	Hynix H5GC8H24MJR-R0C

Function	ROM_SLK_D4		ROM_SI_D3		ROM_SO_C4	
	R7902	R7932	R7933	R7934	R7950	R7935
SORx_EXPOSED	100K	100K	NA	100K	NA	100K

ROM_SLK	ROM_SI	ROM_SO	Function
M(0.9V)	L	L	as below picture

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

STRAP3	STRAP4	STRAP5	Function
L	L	L	as Table 5.6

STRAP3	STRAP4	STRAP5	Function
R7928	R7939	R7929	R7940	R7945	R7953
SMB ALT ADDR DEVID SEL PCIE CFG VGA DEVICE	NA	100K	NA	100K	NA	100K

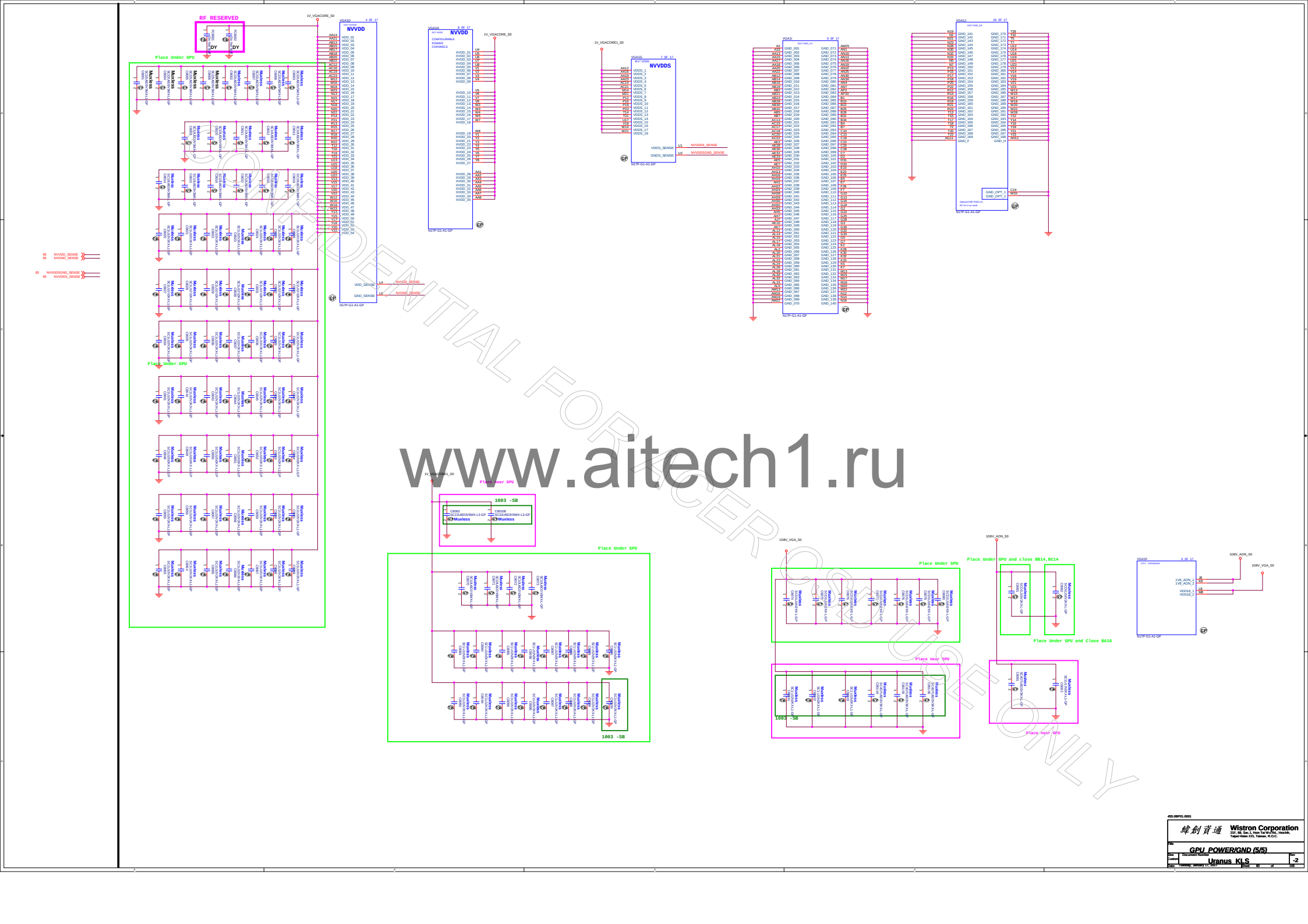
455.0BP01.0001

蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., HsiChih, Taipei Hsien 221, Taiwan, R.O.C.

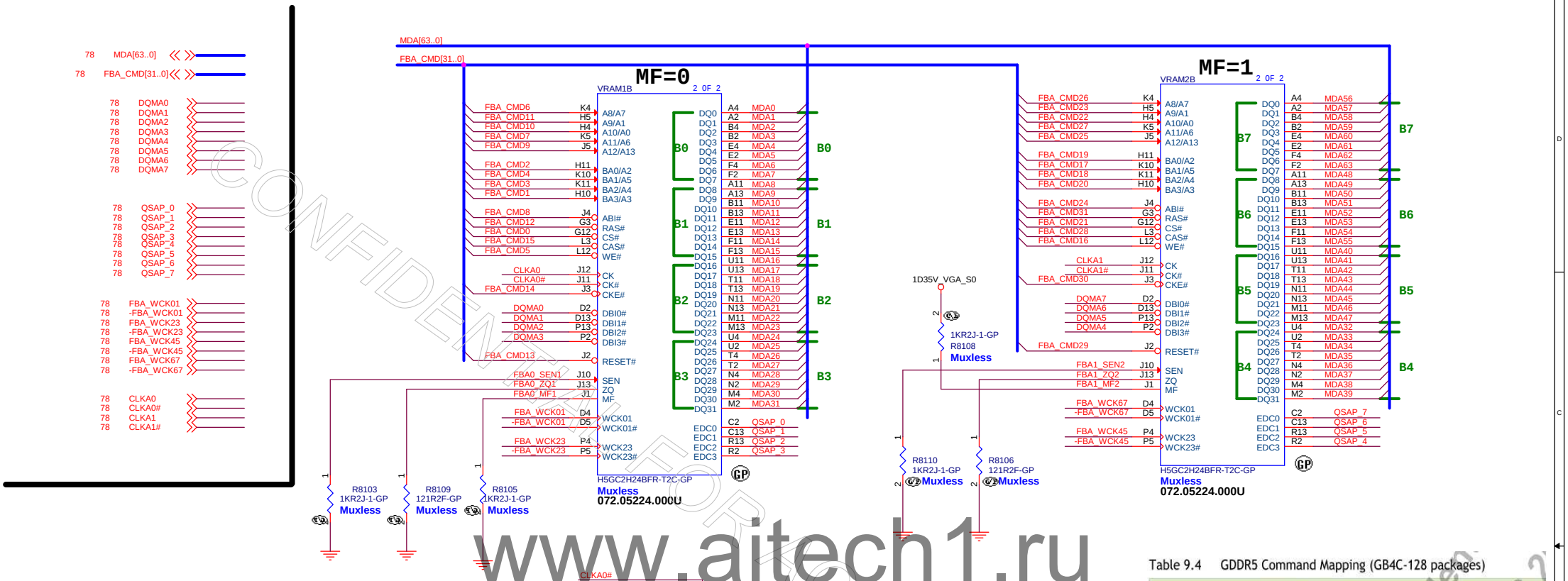
GPU_GPIO/STRAP

Size	Document Number	Rev
A1	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 79 of 105



455.08P01.0001	緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: GPU_POWER/GND (5/5)		
Size: Custom	Document Number: Uranus_KLS	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 80 of 105	



GDDR5 Data Mapping

BYTE0 (BYTE4)		BYTE1 (BYTE5)		BYTE2 (BYTE6)		BYTE3 (BYTE7)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ32)	DQ8	DQ16 (DQ40)	DQ16	DQ8 (DQ48)	DQ24	DQ0 (DQ56)
DQ1	DQ25 (DQ33)	DQ9	DQ17 (DQ41)	DQ17	DQ9 (DQ49)	DQ25	DQ1 (DQ57)
DQ2	DQ26 (DQ34)	DQ10	DQ18 (DQ42)	DQ18	DQ10 (DQ50)	DQ26	DQ2 (DQ58)
DQ3	DQ27 (DQ35)	DQ11	DQ19 (DQ43)	DQ19	DQ11 (DQ51)	DQ27	DQ3 (DQ59)
DQ4	DQ28 (DQ36)	DQ12	DQ20 (DQ44)	DQ20	DQ12 (DQ52)	DQ28	DQ4 (DQ60)
DQ5	DQ29 (DQ37)	DQ13	DQ21 (DQ45)	DQ21	DQ13 (DQ53)	DQ29	DQ5 (DQ61)
DQ6	DQ30 (DQ38)	DQ14	DQ22 (DQ46)	DQ22	DQ14 (DQ54)	DQ30	DQ6 (DQ62)
DQ7	DQ31 (DQ39)	DQ15	DQ23 (DQ47)	DQ23	DQ15 (DQ55)	DQ31	DQ7 (DQ63)
DBI0	DBI3 (DBI4)	DBI1	DBI2 (DBI5)	DBI2	DBI1 (DBI6)	DBI3	DBI0 (DBI7)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC6)	EDC3	EDC0 (EDC7)

GDDR5 CLK Mapping

WCK01	WCK23 (WCK45)	WCK23	WCK01 (WCK67)
WCK01#	WCK23# (WCK45#)	WCK23#	WCK01# (WCK67#)
CK	CK		
CK#	CK#		

Others

MF	MF	SEN	SEN
ZQ	ZQ	RESET#	RESET#

Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

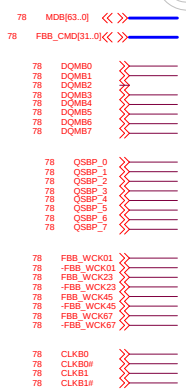
455.0BP01.0001

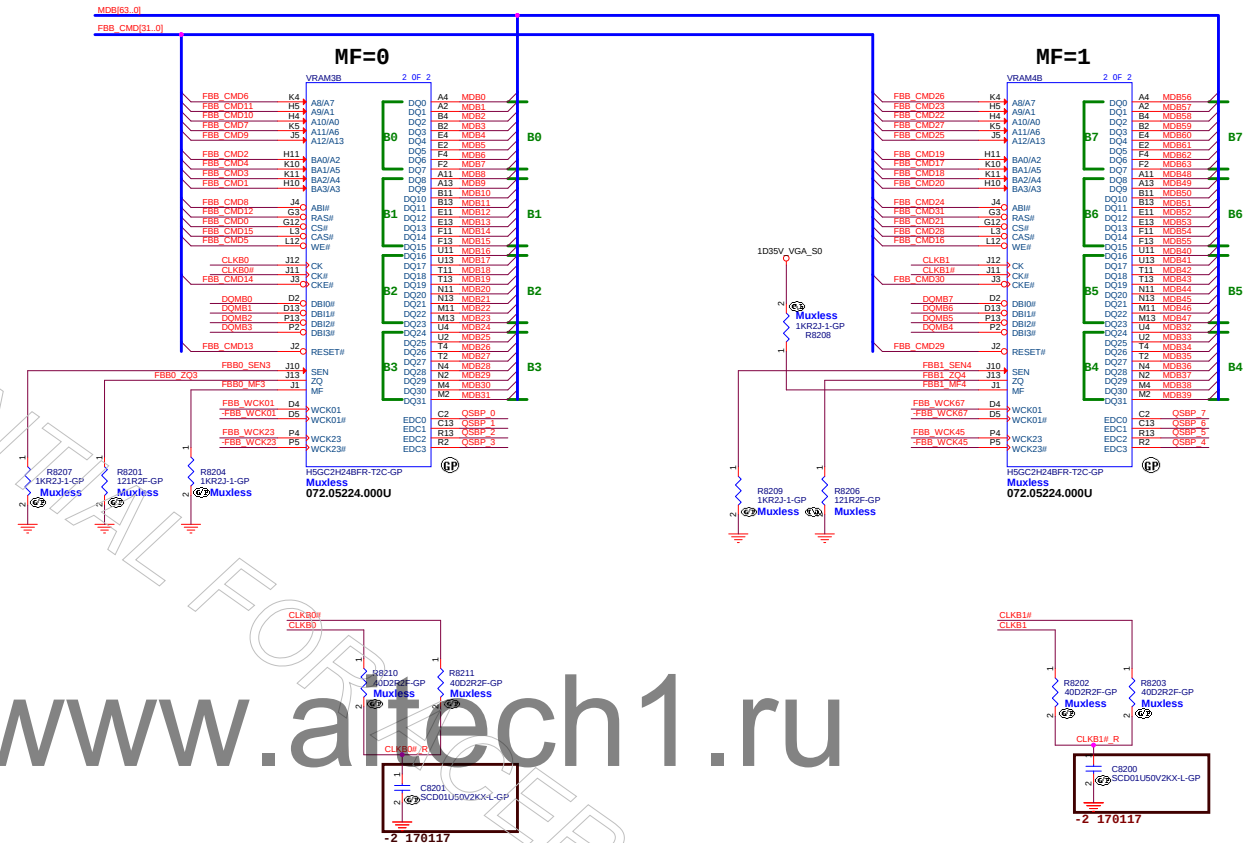
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM 1,2 (1/4)

Size: Custom | Document Number: Uranus_KLS | Rev: -2

Date: Tuesday, January 17, 2017 | Sheet 81 of 105





GDDR5 Data Mapping							
BYTE0 (BYTE4)		BYTE1 (BYTE5)		BYTE2 (BYTE6)		BYTE3 (BYTE7)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ32)	DQ8	DQ16 (DQ40)	DQ16	DQ8 (DQ48)	DQ24	DQ0 (DQ56)
DQ1	DQ25 (DQ33)	DQ9	DQ17 (DQ41)	DQ17	DQ9 (DQ49)	DQ25	DQ1 (DQ57)
DQ2	DQ26 (DQ34)	DQ10	DQ18 (DQ42)	DQ18	DQ10 (DQ50)	DQ26	DQ2 (DQ58)
DQ3	DQ27 (DQ35)	DQ11	DQ19 (DQ43)	DQ19	DQ11 (DQ51)	DQ27	DQ3 (DQ59)
DQ4	DQ28 (DQ36)	DQ12	DQ20 (DQ44)	DQ20	DQ12 (DQ52)	DQ28	DQ4 (DQ60)
DQ5	DQ29 (DQ37)	DQ13	DQ21 (DQ45)	DQ21	DQ13 (DQ53)	DQ29	DQ5 (DQ61)
DQ6	DQ30 (DQ38)	DQ14	DQ22 (DQ46)	DQ22	DQ14 (DQ54)	DQ30	DQ6 (DQ62)
DQ7	DQ31 (DQ39)	DQ15	DQ23 (DQ47)	DQ23	DQ15 (DQ55)	DQ31	DQ7 (DQ63)
DBI0	DBI3 (DBI4)	DBI1	DBI2 (DBI5)	DBI2	DBI1 (DBI6)	DBI3	DBI0 (DBI7)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC6)	EDC3	EDC0 (EDC7)

GDDR5 CLK Mapping			
WCK01	WCK23 (WCK45)	WCK23	WCK01 (WCK67)
WCK01#	WCK23# (WCK45#)	WCK23#	WCK01# (WCK67#)
CK	CK		
CK#	CK#		

Others			
MF	MF	SEN	SEN
ZQ	ZQ	RESET#	RESET#

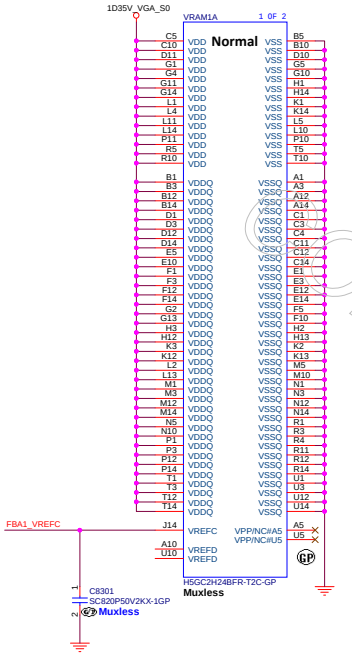
Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

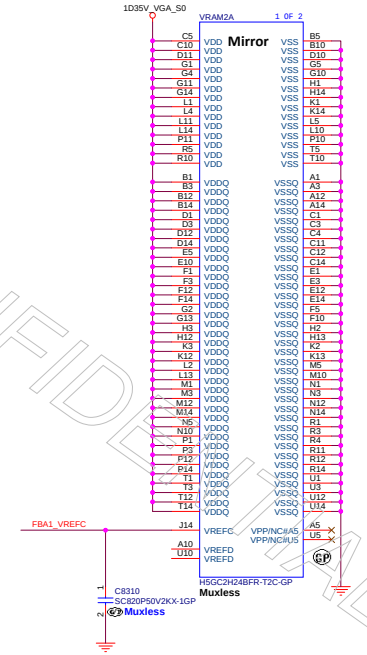
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

455.0BP01.0001

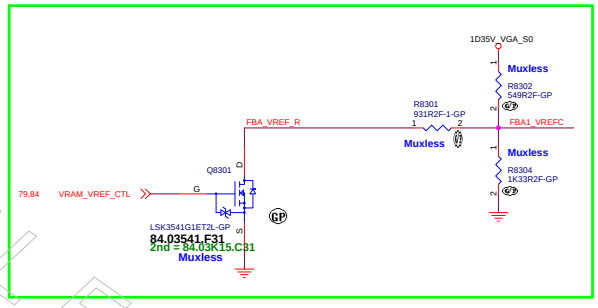
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM 3,4 (2/4)		
Size: Custom	Document Number: Uranus_KLS		Rev: -2
Date: Tuesday, January 17, 2017	Sheet 82 of 105		

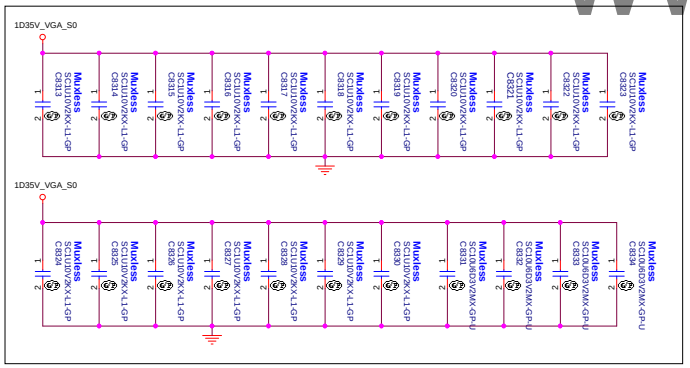




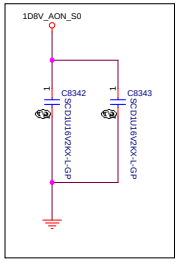
CLOSE TO VRAM



FOR VRAM1/ VRAM2

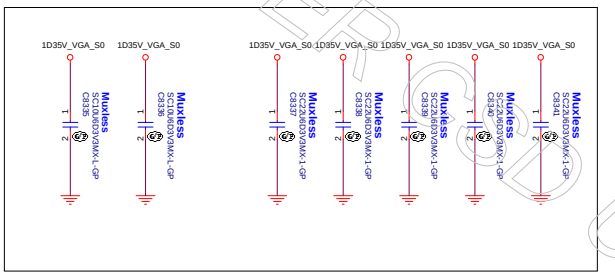


UNDER THE MEMORY



UNDER THE MEMORY

FOR VRAM1/ VRAM2



CLOSE TO THE MEMORY

455.08P01.0001

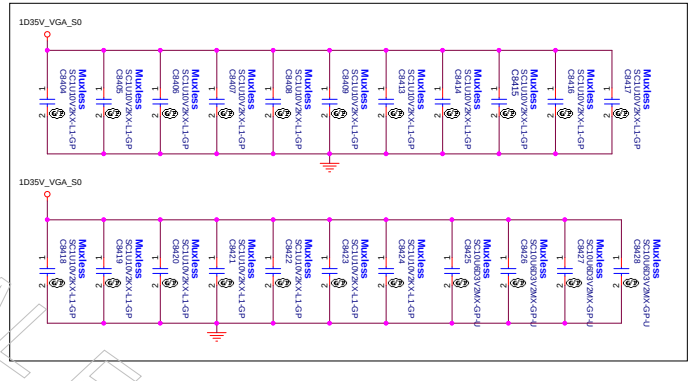
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM 5,6 (3/4)***

Size: A2 | Document Number: Uranus_KLS | Rev: -2

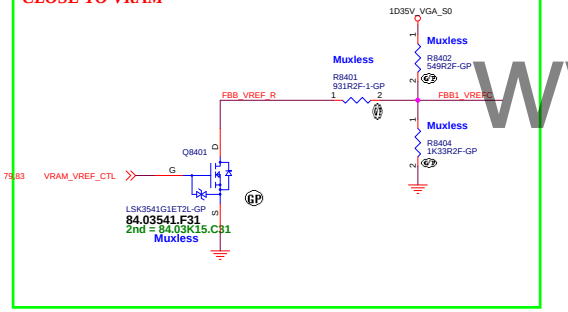
Date: Tuesday, January 17, 2017 | Sheet 83 of 105

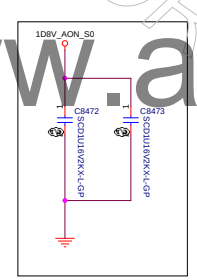
FOR VRAM3/ VRAM4



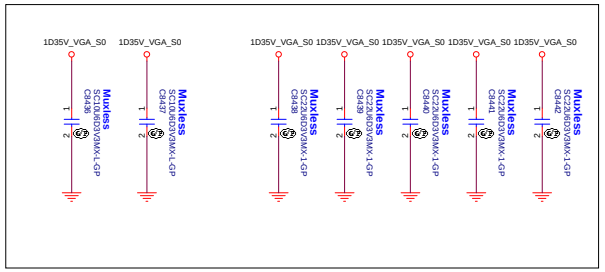
UNDER TO THE MEMORY

CLOSE TO VRAM





UNDER THE MEMORY



CLOSE TO THE MEMORY

455.0BP01.0001

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA Power A

Size: A2 | Document Number: Uranus_KLS | Rev: -2

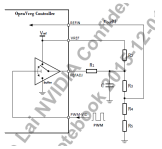
Date: Tuesday, January 17, 2017 | Sheet 84 of 105

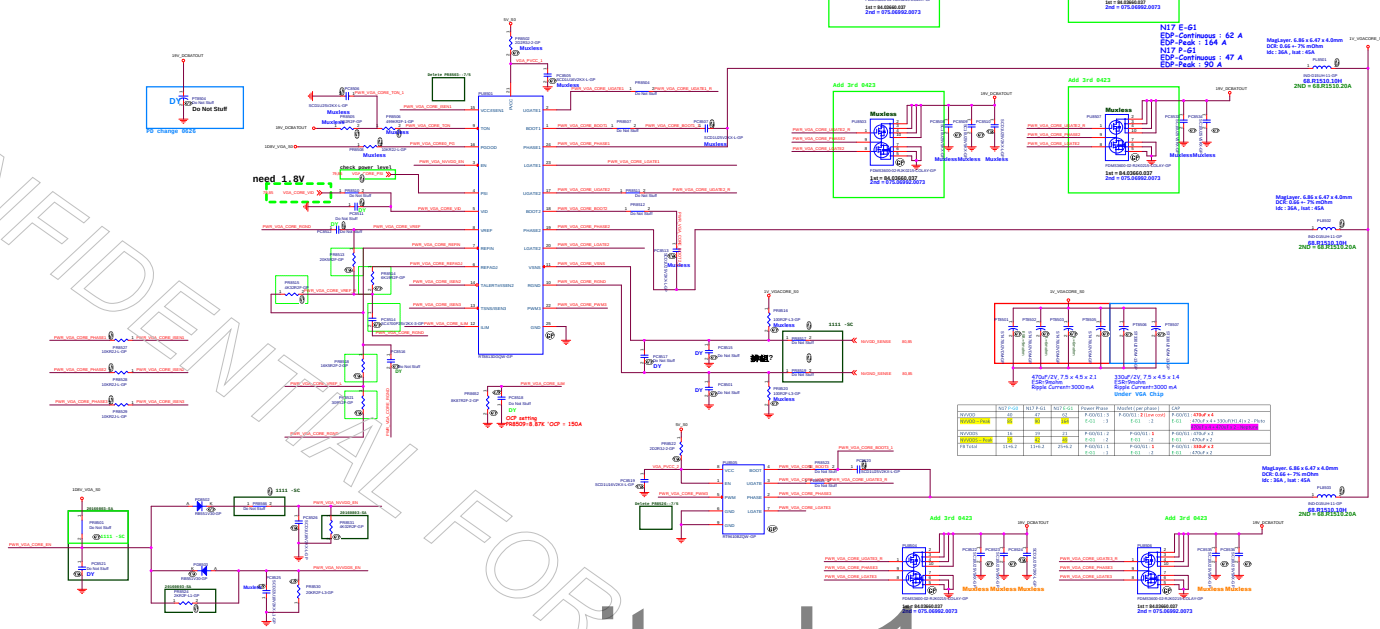
VGA : N17E-G1
Config : B
EDP-Continuous : 58A
EDP-Peak : 136A

CHECK SPEC

Table 7.8 PWM-VID Spec and Component Values

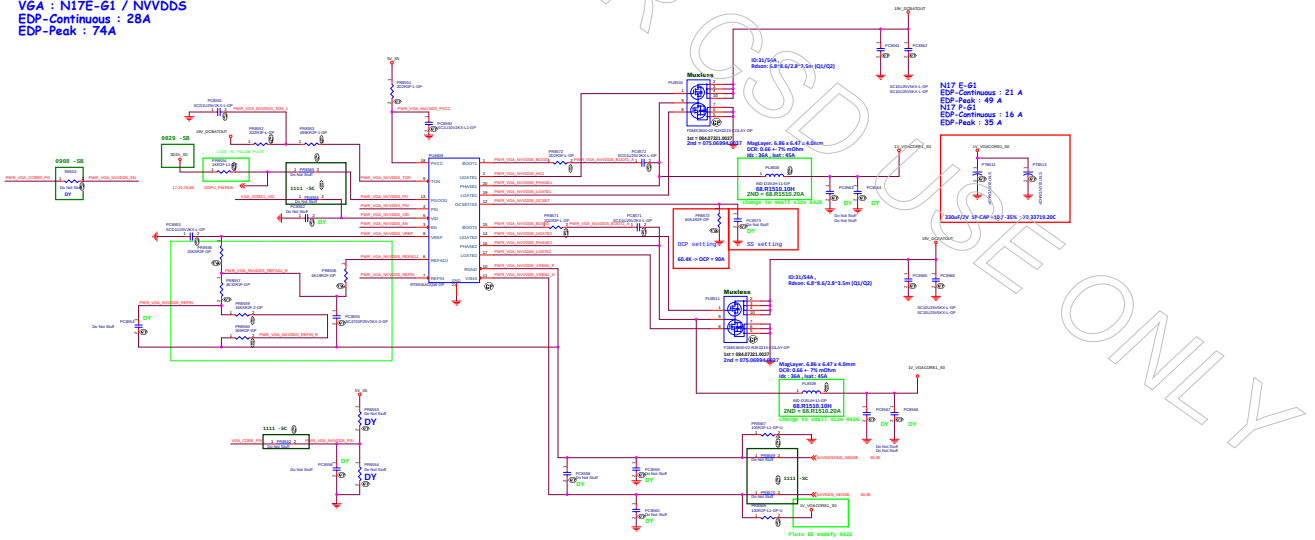
PWM-VID Specification		
	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7





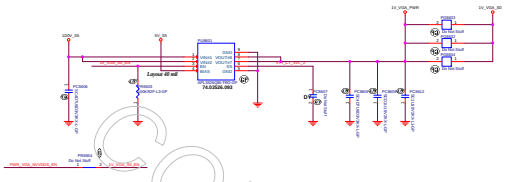
RT8816A For NVVDDS

VGA : N17E-G1 / NVVDDS
EDP-Continuous : 28A
EDP-Peak : 74A

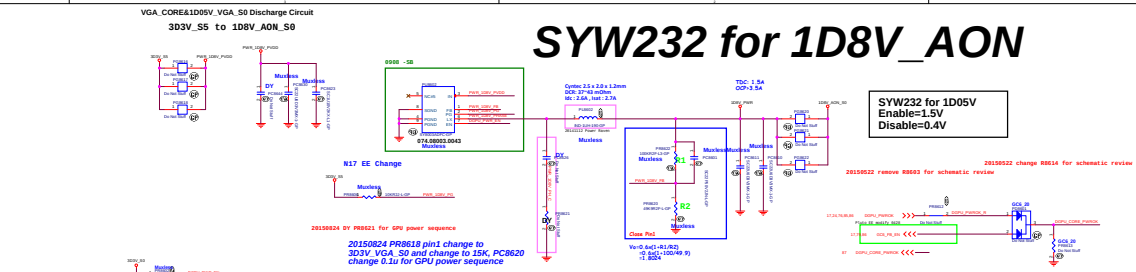


Wistron Corporation	
VGA Power B	
Uranus KLS	-2

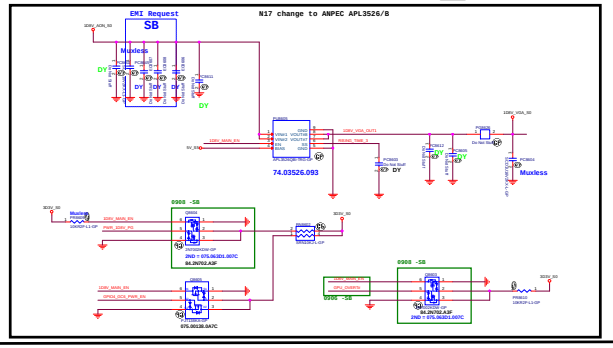
APL3526QB for 1V_VGA_S0



SYW232 for 1D8V_AON



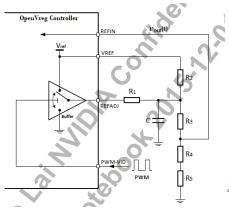
SYW232 for 1D8V_MAIN

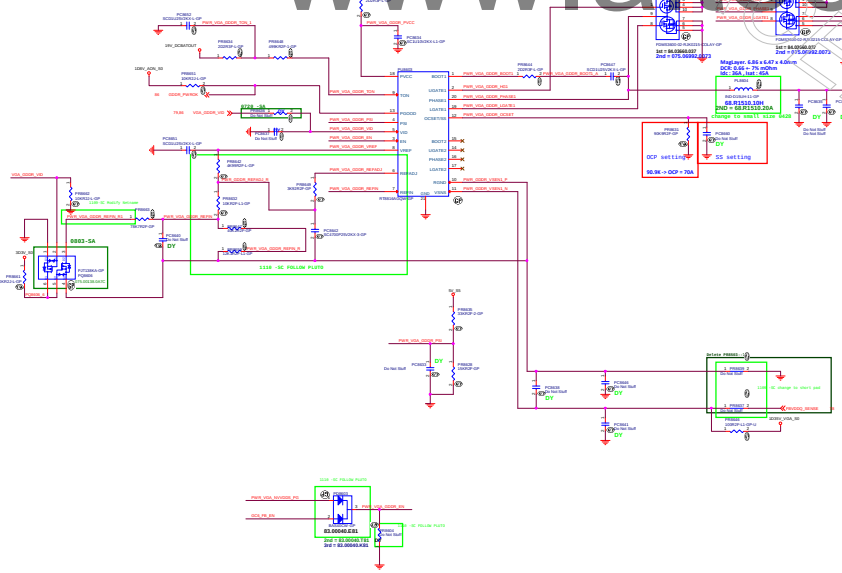


RT8816A for PWR_VGA_GDDR

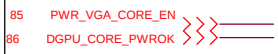
Table 7.8 PWM-VID Spec and Component Values

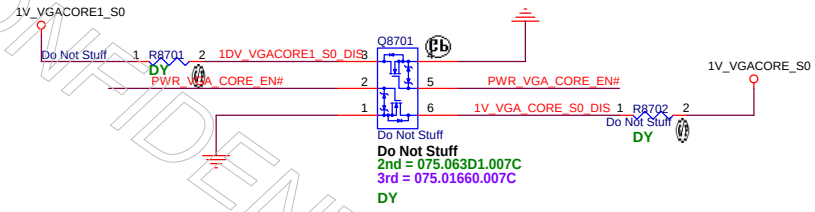
PWM-VID Specification		
	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.3/0
C	nF	4.7

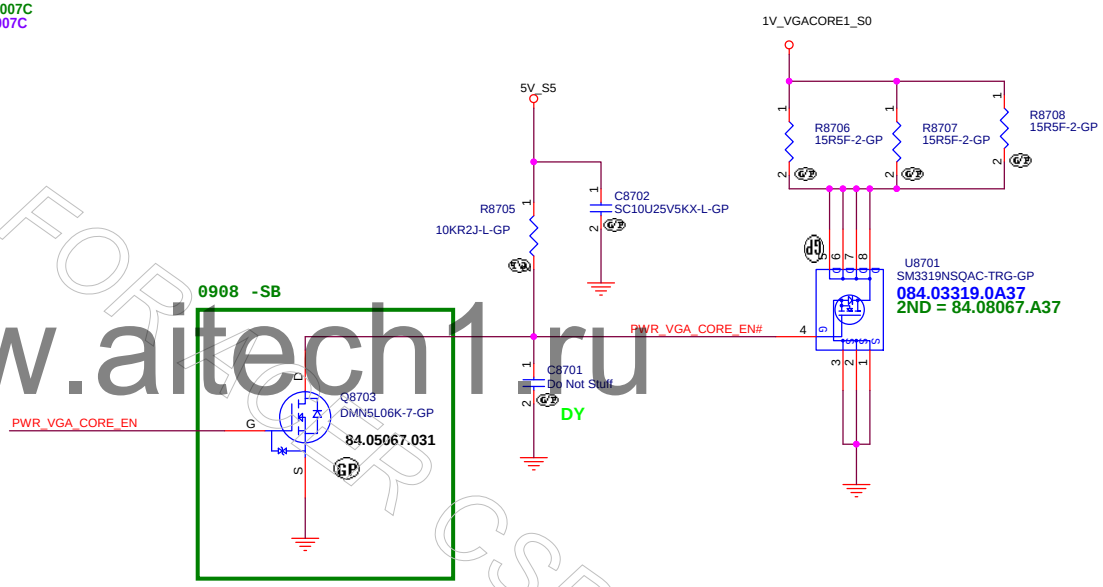


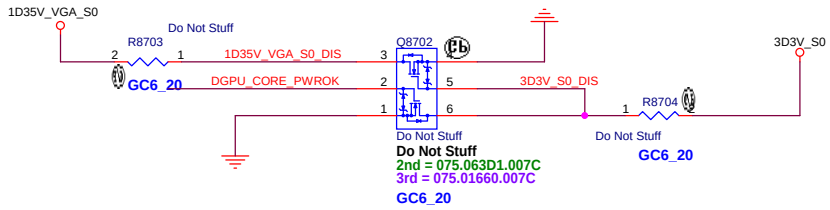


Wistron Corporation
DISCRETE VGA POWER
Uranus K1.S
-2









SKU1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Discharge***

Size	Document Number	Rev
A3	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 87 of 105

SKU1

緯創資通

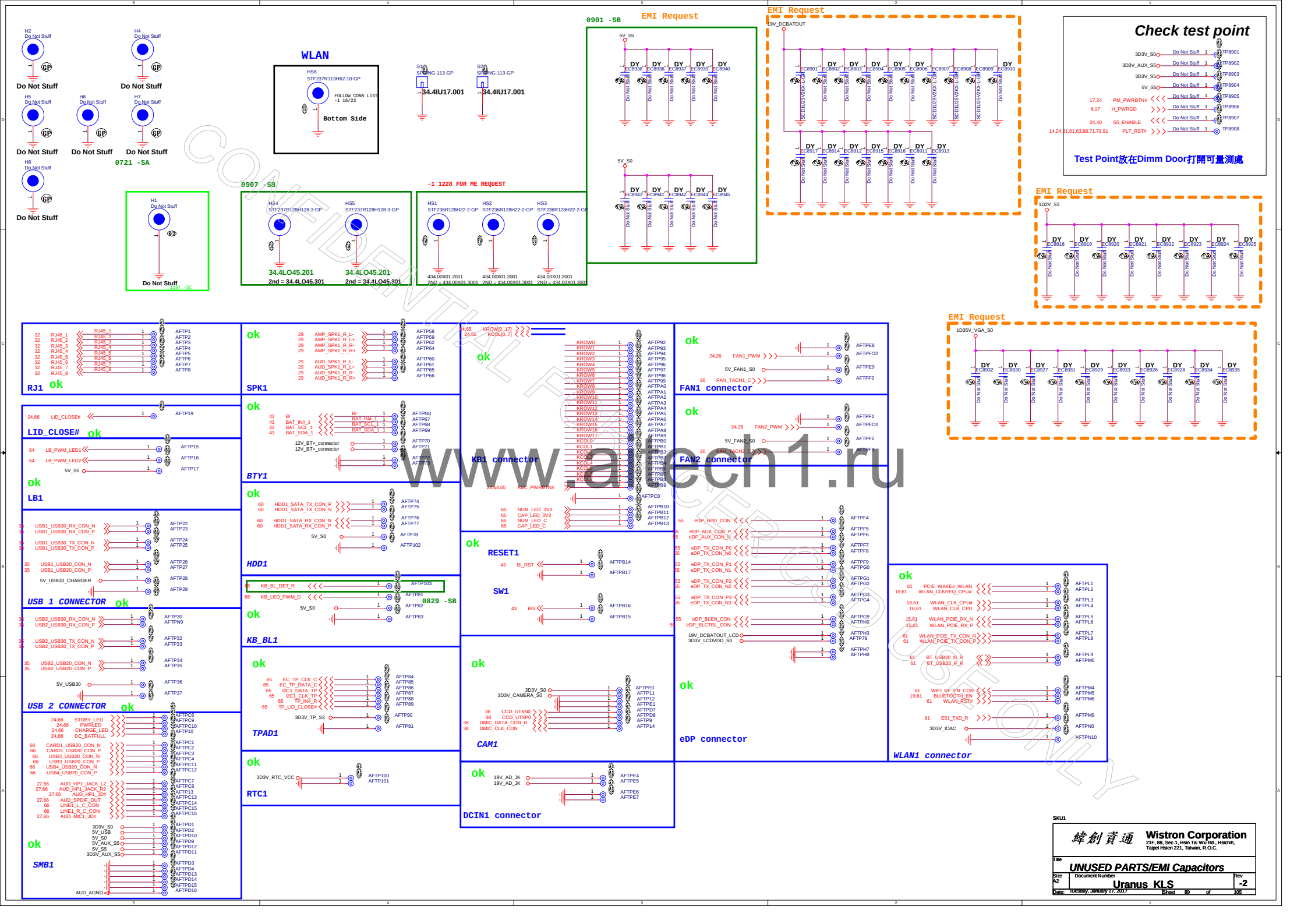
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 88 of 105



SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

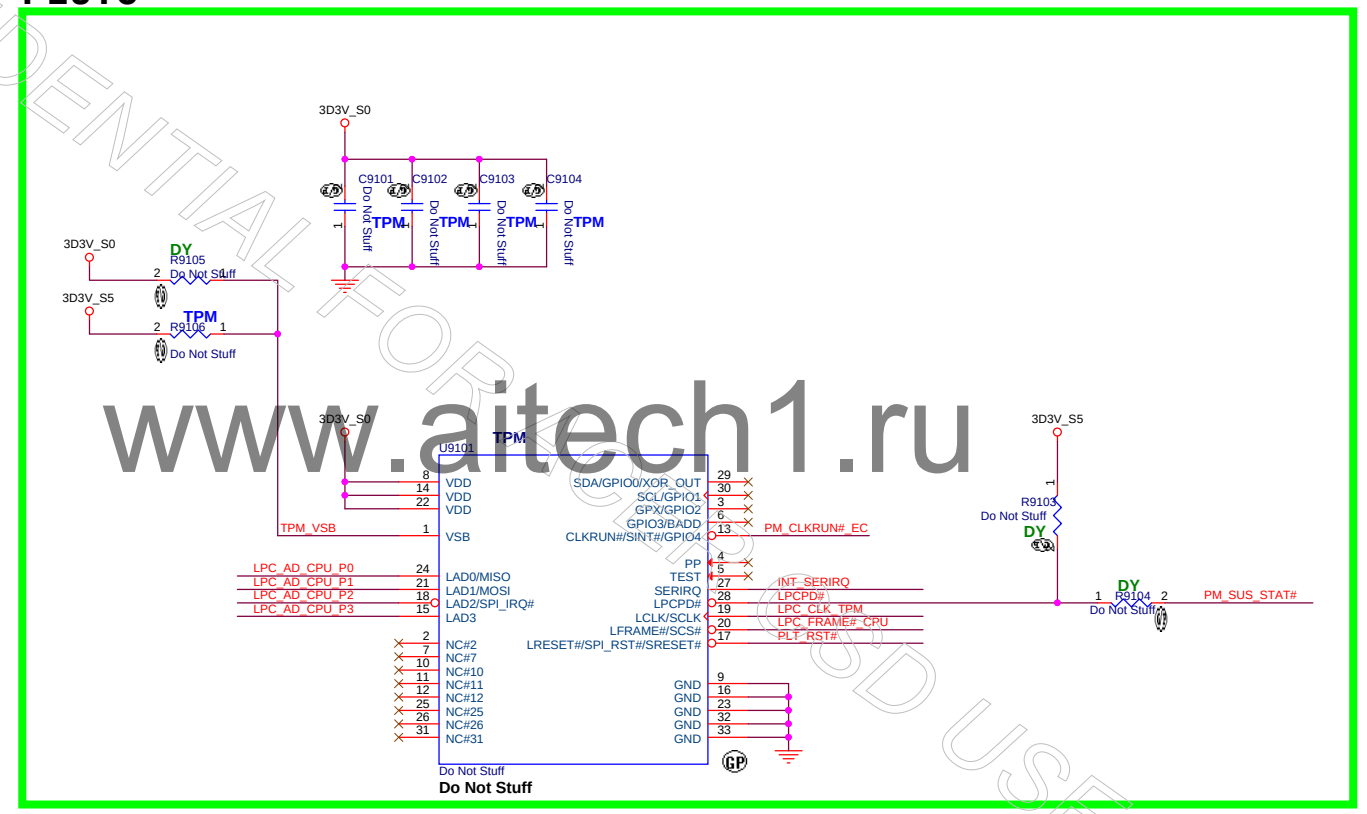
Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 90 of 105

18,24,68 LPC_FRAME#_CPU
18,24,68 INT_SERIRQ
18 PM_SUS_STAT#
18 LPC_CLK_TPM
4,24,31,61,63,68,71,79,89 PLT_RST#
17,24 PM_CLKRUN#_EC

18,24,68 LPC_AD_CPU_P0
18,24,68 LPC_AD_CPU_P1
18,24,68 LPC_AD_CPU_P2
18,24,68 LPC_AD_CPU_P3

PLUTO

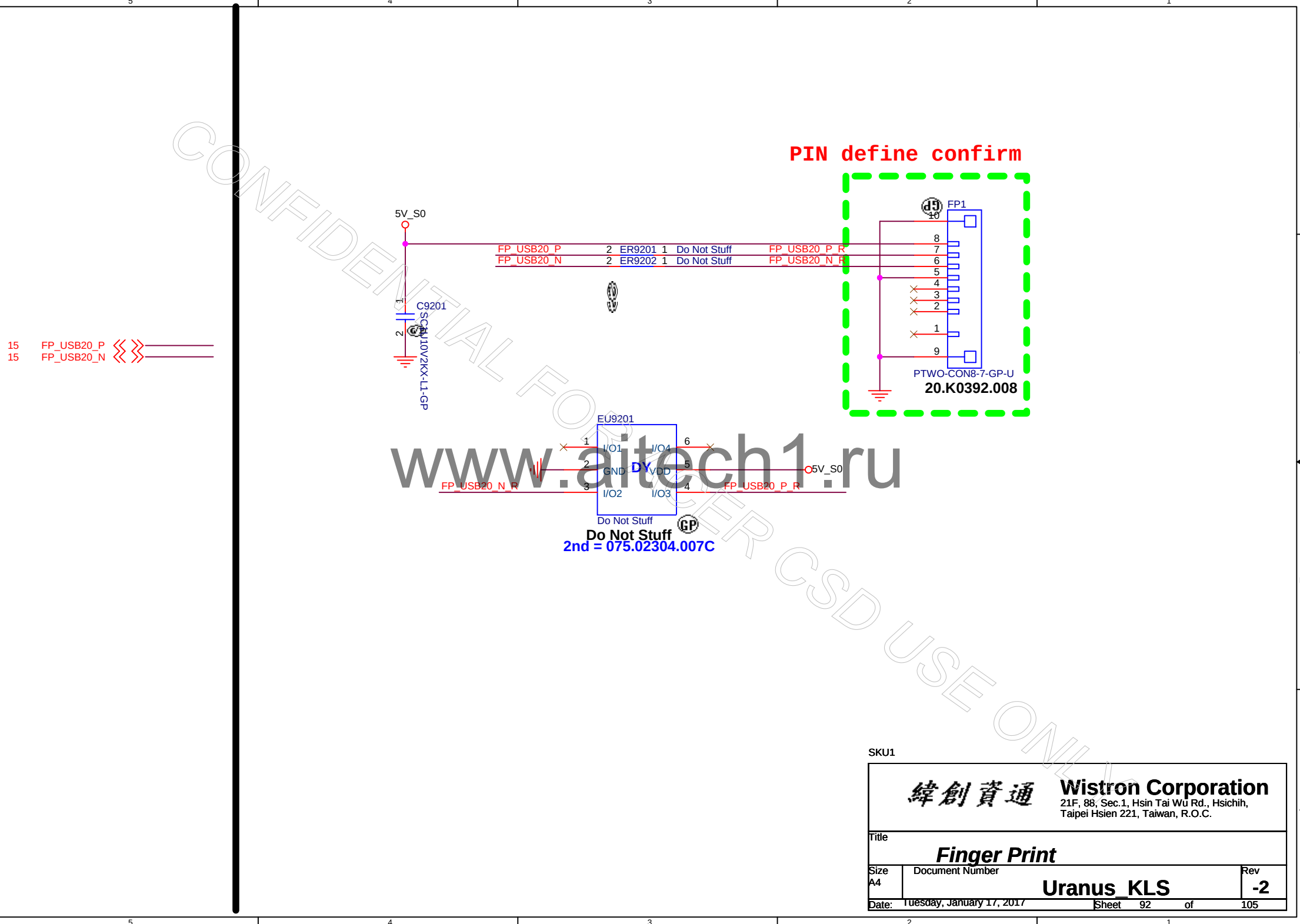


Do Not Stuff

SKU1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***TPM/NPCT650***	
Size A3	Document Number **Uranus_KLS**	Rev **-2**
Date: Tuesday, January 17, 2017	Sheet 91 of 105	


PIN define confirm
5V_S0
FP_USB20_P
FP_USB20_N
2 ER9201 1 Do Not Stuff
2 ER9202 1 Do Not Stuff
FP_USB20_P_R
FP_USB20_N_R
C9201
SC2AU10V2KX-L1-GP
FP1
PTWO-CON8-7-GP-U
20.K0392.008
EU9201
I/O1
GND
I/O2
I/O4
VDD
I/O3
5V_S0
FP_USB20_N_R
FP_USB20_P_R
Do Not Stuff
Do Not Stuff
2nd = 075.02304.007C
15 FP_USB20_P
15 FP_USB20_N
CONFIDENTIAL FOR WISTRON CSD USE ONLY
www.aitech1.ru
SKU1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Finger Print
Size A4
Document Number
Uranus_KLS
Rev -2
Date: Tuesday, January 17, 2017
Sheet 92 of 105

SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 93 of 105

SKU1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
C	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 94 of 105

SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 95 of 105

SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 96 of 105

SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU_CFG_CFG STRAP

Size	Document Number	Rev
A	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 97 of 105

SKU1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU_CFG_CFG STRAP

Size	Document Number	Rev
A	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 98 of 105

SKU1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_XDP***

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 99 of 105

SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Table of Content

Size	Document Number	Rev
A	**Uranus_KLS**	**-2**
Date: Tuesday, January 17, 2017	Sheet 100 of 105	

SKU1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

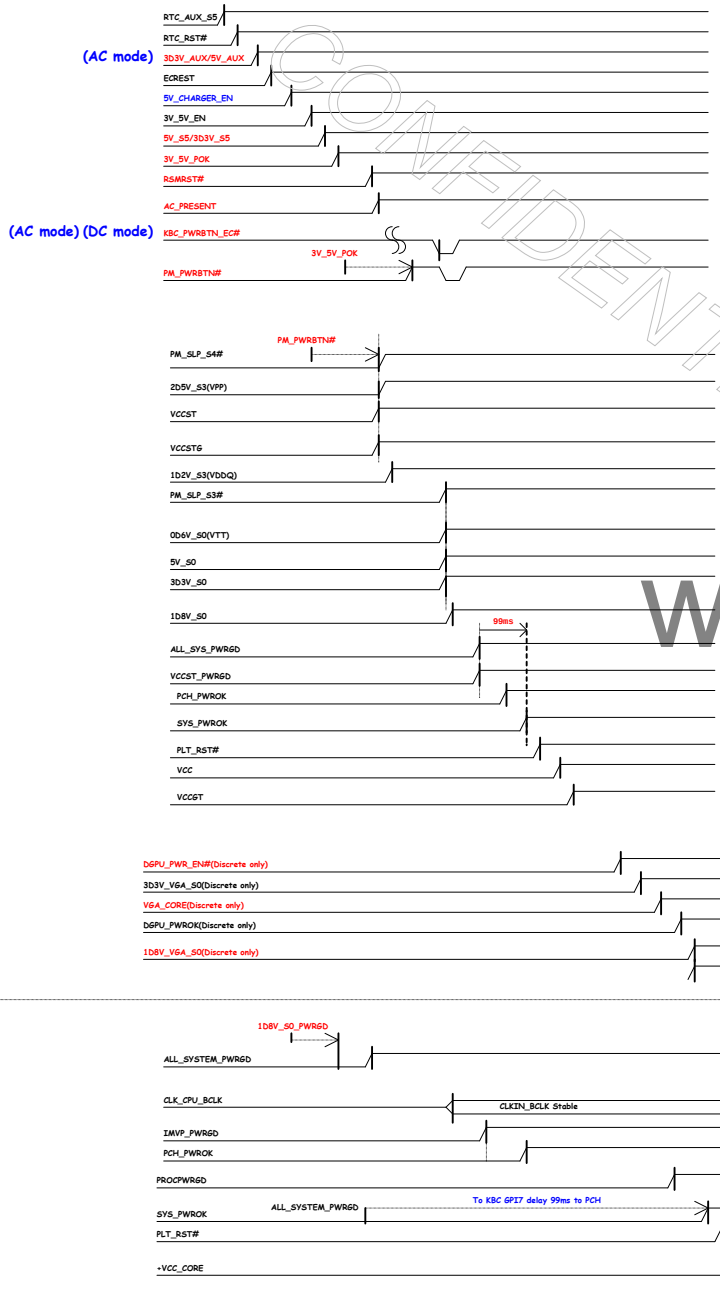
Title

Change History

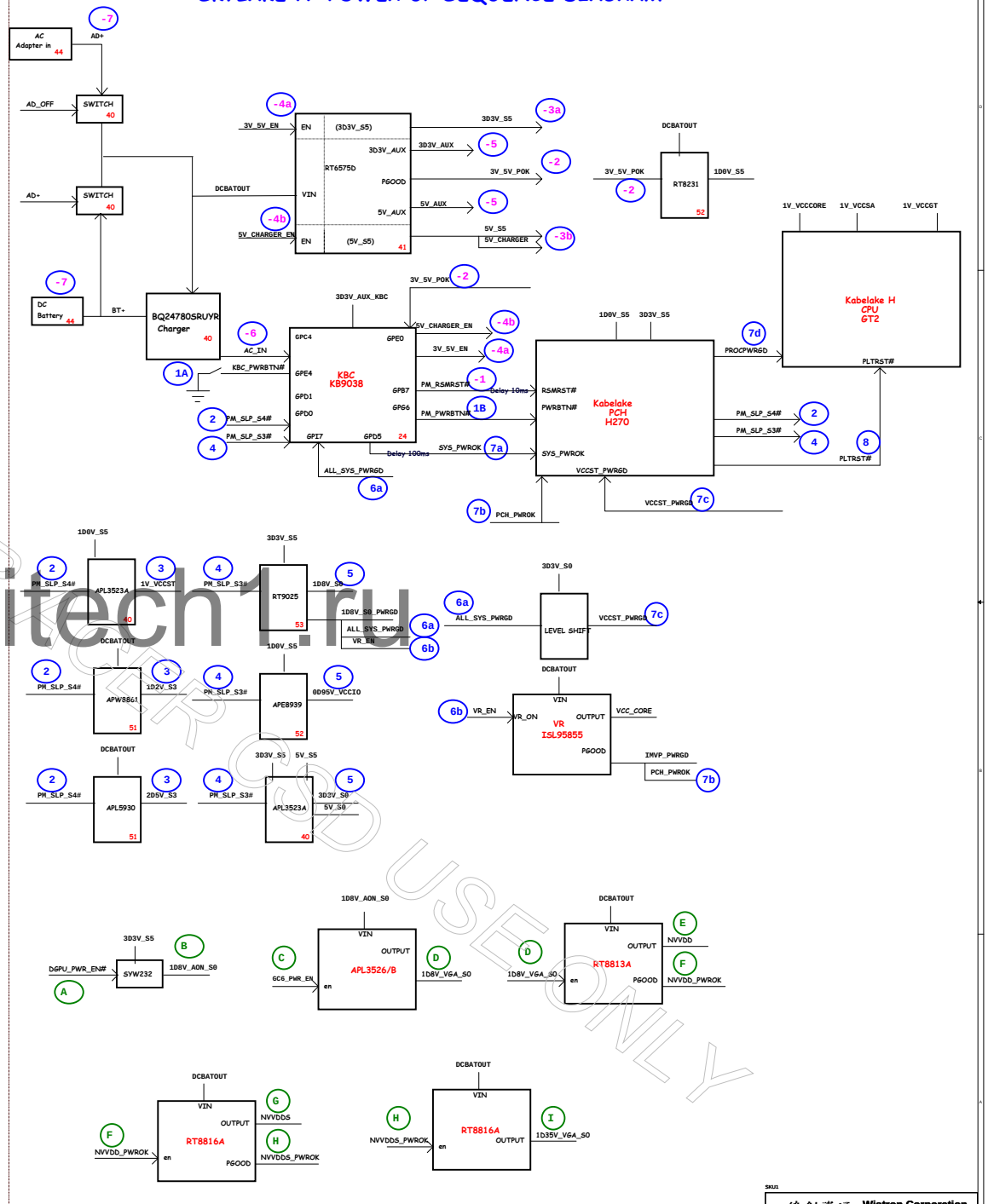
Size	Document Number	Rev
A	**Uranus_KLS**	**-2**

Date: Tuesday, January 17, 2017 Sheet 101 of 105

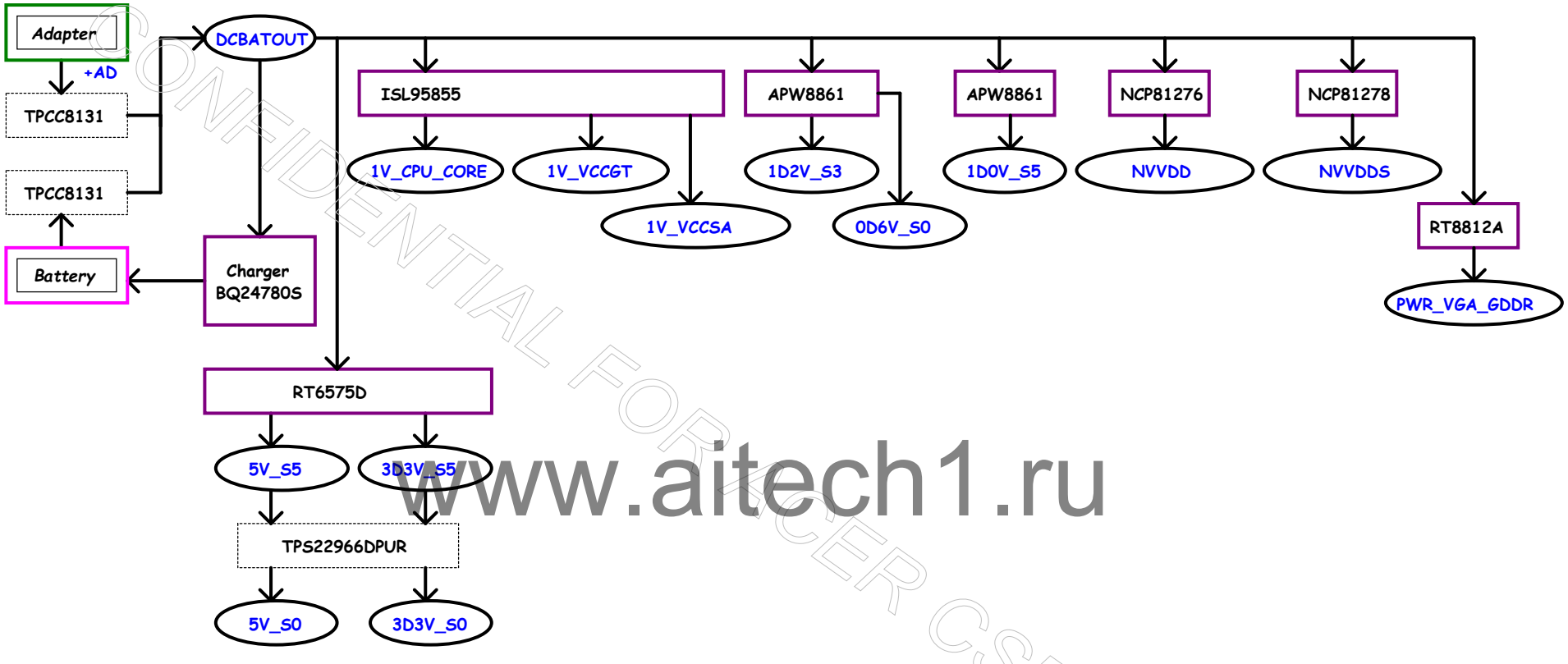
Intel-Power Up Sequence



SKYLAKE H POWER UP SEQUENCE DIAGRAM



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Power Sequence	
Size: A1	Document Number: Uranus_KLS
Rev: -2	
Date: Tuesday, January 17, 2017	Sheet 100 of 105



Regulator | LDO | Switch

SKU1

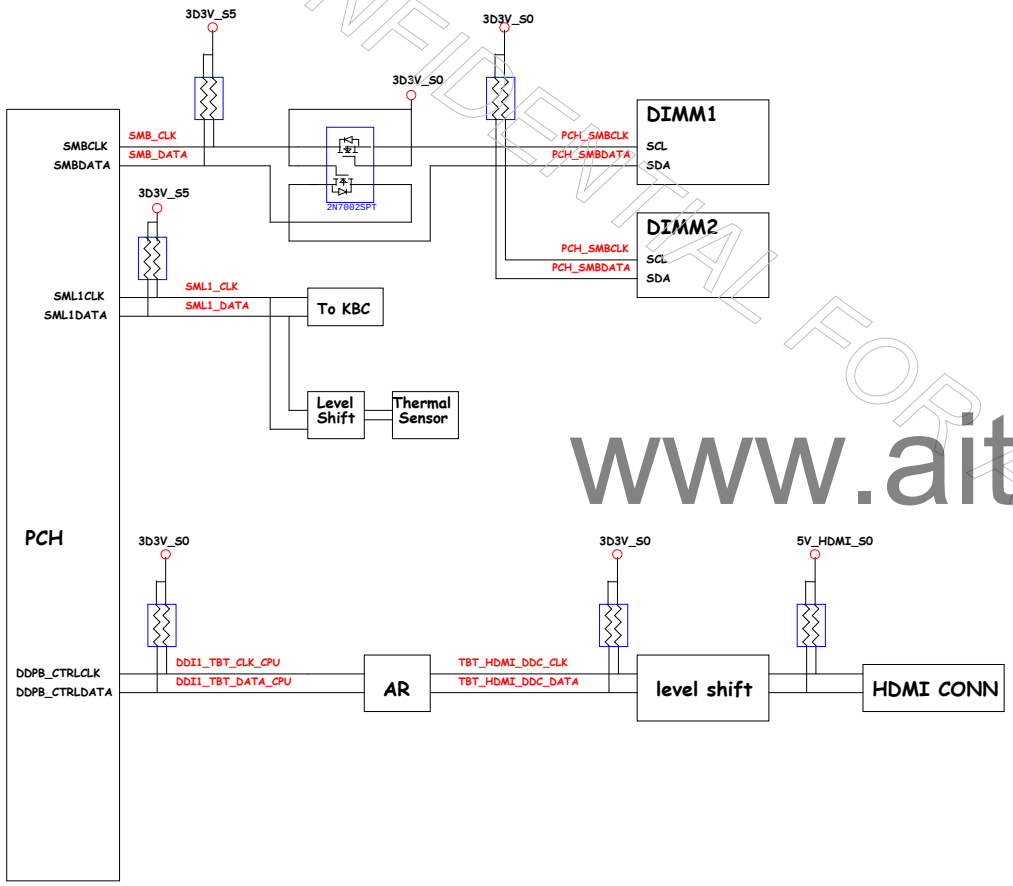
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

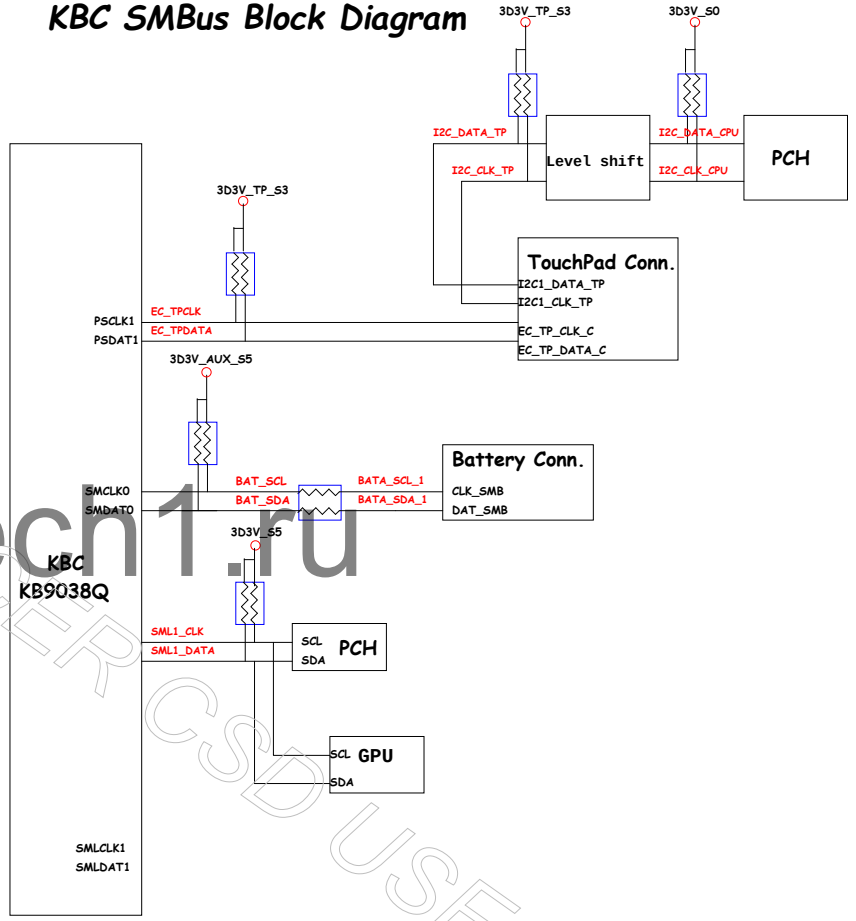
Size	Document Number	Rev
A3	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 103 of 105

PCH SMBus Block Diagram



KBC SMBus Block Diagram



SKU1

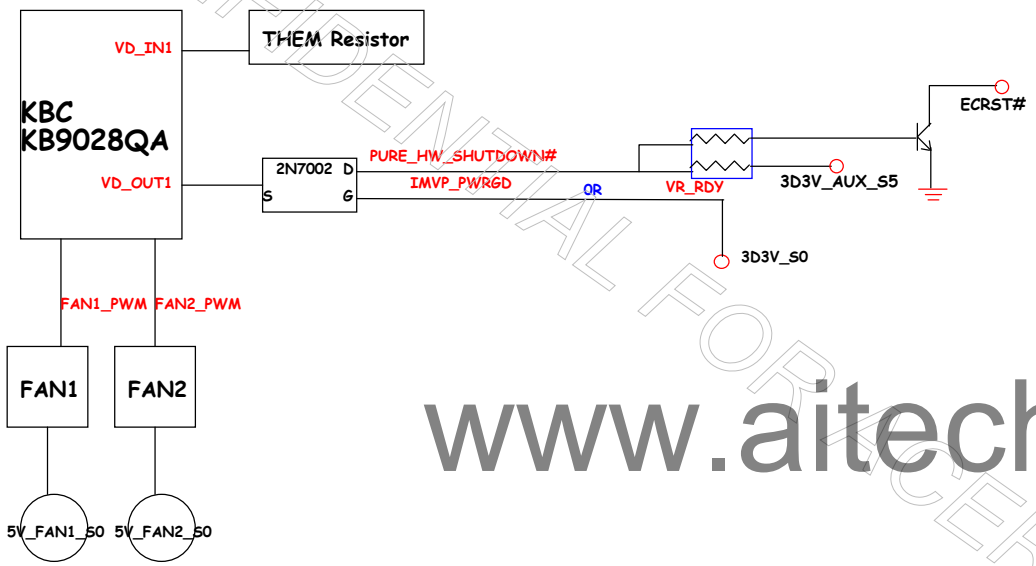
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS BLOCK DIAGRAM

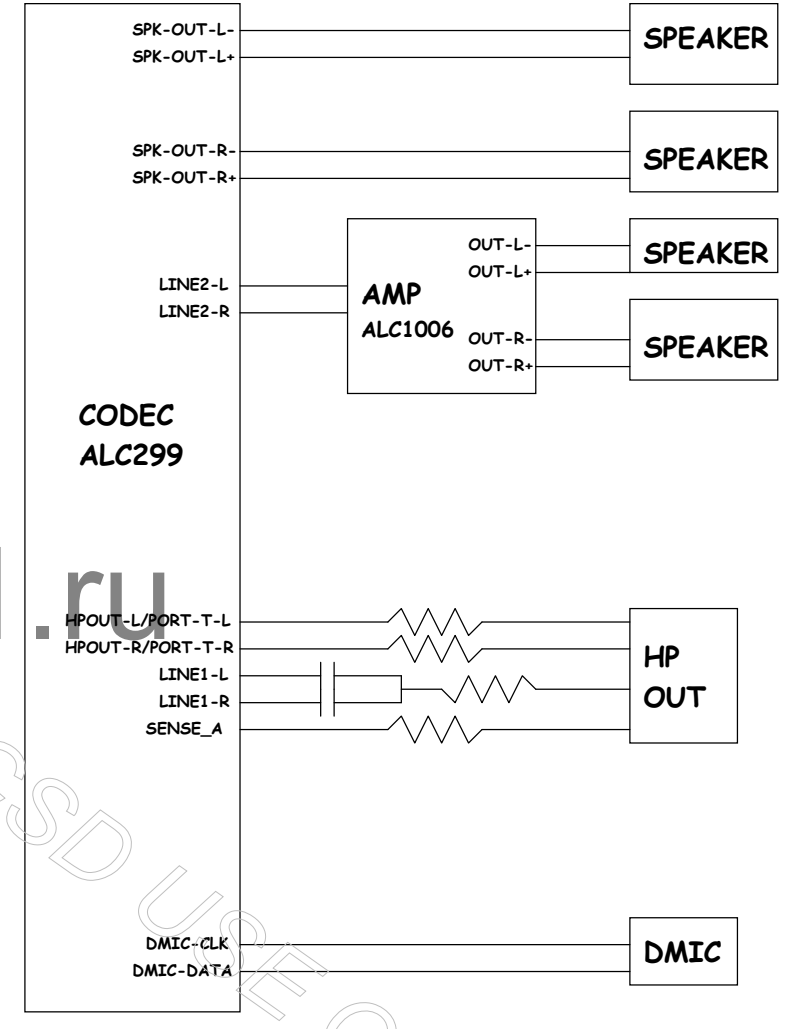
Size	Document Number	Rev
A2	Uranus_KLS	-2

Date: Tuesday, January 17, 2017 Sheet 104 of 105

Thermal Block Diagram



Audio Block Diagram



SKU1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Thermal /AUDIO Block Diagram		
Size: A3	Document Number: Uranus_KLS	Rev: -2
Date: Tuesday, January 17, 2017	Sheet 105 of 105	